Thesis Proposal – Hardware In the Loop (HiL)

GENERAL INFORMATIONS

- **Duration:** 6-8 months
- **Timing:** 2021-2022
- **Site:** PWT's offices (Turin)
- **Compensation:** Meals, Travel exp.

CONTACTS:

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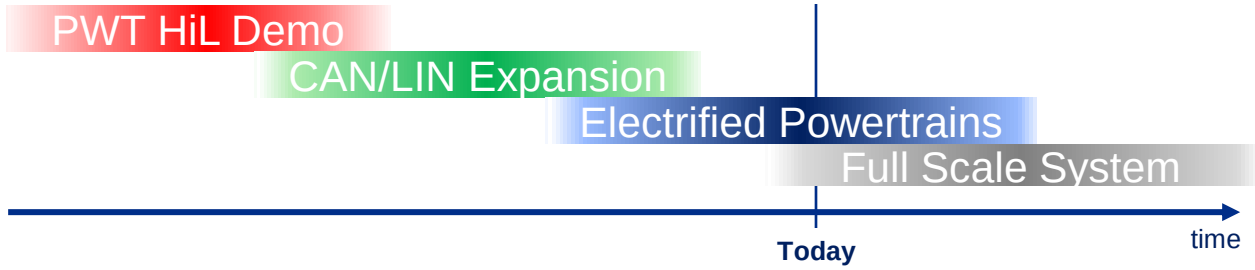
DESCRIPTION:

Powertech Engineering is a leading company in engineering services for powertrain simulation, working with several world-class automotive OEMs.

PWT is increasing its facilities and investments in the field of Hardware-In-the-Loop systems for ECU testing, validation and virtual calibration. In the past years, PWT developed several HiL applications with production ECUs both for conventional and electrified powertrain. In this context, PWT is further developing its methodologies for power electronics and electric motors modelling for FPGA application.

Furthermore, in the second half of 2021 PWT's HiL facilities will be expanded with a Full Scale System-HiL able to handle modern multi-node automotive control units network.



Thesis Proposal #1 – Flux Based PMSM FPGA Model

Background:

At the moment PWT relies on dSPACE current-based PMSM models machines for Real Time FPGA applications. From previous internal activities flux linkage models were found to be more accurate and stable

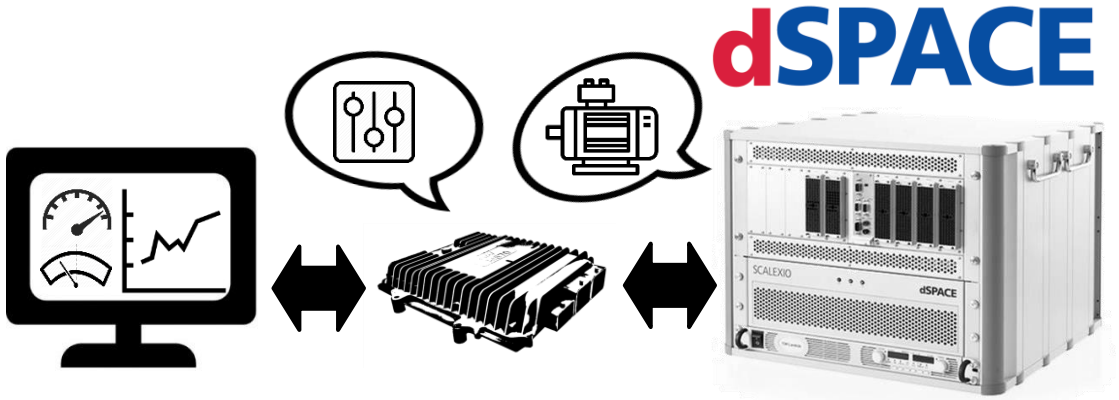
Tasks:

The student will be in charge of:

- Develop PMSM Flux-Linkage model for FPGA applications
  - Processor interface
  - FPGA model
- Benchmark with existing current model

Hardware:

- dSPACE based HiL System
  - SCALEXIO XEON E3-1275v6
  - DS2655 FPGA Board



Current model

$$L_d \cdot \frac{\mathrm{d}i_d}{\mathrm{d}t} = v_d - R_s \cdot i_d + \omega \cdot L_q \cdot i_q$$

$$L_q \cdot \frac{\mathrm{d}i_q}{\mathrm{d}t} = v_q - R_s \cdot i_q - \omega \cdot (L_d \cdot i_d + \lambda_m)$$

Flux-linkage model

$$\frac{\mathrm{d}\lambda_d}{\mathrm{d}t} = v_d - R_s \cdot i_d + \omega \cdot \lambda_q$$

$$\frac{\mathrm{d}\lambda_q}{\mathrm{d}t} = v_q - R_s \cdot i_q - \omega \cdot \lambda_d$$

Thesis Proposal #2 – Setup of a full scale System HiL

Background:

PWT is investing in new facilities for HiL simulations stepping from a desktop-based system to a full-scale system HiL able to handle modern multi-note automotive control system.

Tasks:

The student will be in charge of:

- System Configuration
  - I/O setup
  - Models interface
  - CAN & LIN Bus communication
- System Commissioning
  - Stimulus tests
  - Closed loop tests

Hardware:

- dSPACE based full scale HiL System
  - SCALEXIO XEON E3-1275v6
  - DS2655 FPGA Board