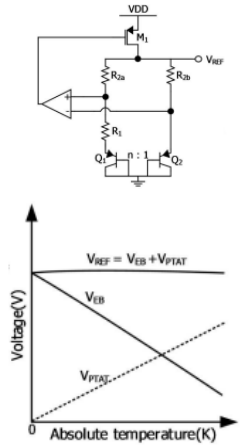
ST Internship proposal

Division	Automotive Division Group
Group	Smart Power Solutions RnD
Title of the Internship Project	Design of ultra low power bandgap voltage reference
Description of the Thesis work (tasks that the student will be performing, objectives of the position)	Study and design of an accurate voltage reference biased in the nA current range for low power applications. Analysis and comparison of different architectural choices in terms of noise, rejection and reference stability across process, voltage and temperature
Field of application and competence development 	The growing market of electric and hybrid vehicles is exponentially increasing the number of electronic equipment inside the cars, moreover such equipment need to be supplied when the car is parked as well for instance for car connectivity and new services such as camera control of the nearby events. Automotive market is asking for extremely low power devices, to reduce overall battery drain and extend car autonomy, keeping same level or even better level of performances, challenging electronic designers. Among all structures, bandgap reference is one of the most critical to be designed in a low current consumption environment, since it is the reference for all supplied voltages, adcs and monitors of the system. In this thesis, we propose the study of different band-gap architectures in available BCD technology, biased with ultra low current, with the aim to identify the most robust one and design a reliable band-gap reference. Student will acquire skills of low power analog design in latest BCD technologies, learning usage of latest CAD simulation tools and methodologies (cadence framework and Simulink among others) together with strong verification skills by mean of PVT and MC analysis.
Profile related to the position	• Basic analog structure knowledge (band-gap reference, current mirrors, operational amplifiers, compensation methods) • Strong knowledge of transistor level analog electronic concepts (noise, matching, offset, bandwidth) • Cadence design suite or equivalent spice simulation experience is a plus
Location	Cornaredo (MI)
Company Tutor	S. Castorina, G. De Agostini
Duration (at least 720 h, 4 months and a half)	6-9 months
Starting Date/Ending Date	
Reimbursements (€) and benefits	800€/month, canteen lunch and transportation from Milano included