NXP Semiconductors Austria, GmbH & Co KG
BL Connectivity & Security, Gratkorn (Austria)

Master Thesis
"Virtual Prototyping of a NFC SW-Defined Radio"

Proposed by:

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Motivations

Near Field Communication (NFC) is an ubiquitous technology with many applications ranging from identification to ticketing, from mobile payment to logistical solutions and, just recently, wireless charging. A considerable amount of analog and digital signal processing is required on all NFC integrated circuits to achieve high performance and reliable communication, while keeping engineering and manufacturing cost low.

Every modem unit of NXP's NFC controllers product family must be able to support multiple communication standards in different operative configurations and environmental conditions. This is achieved today by means of an extensive use of custom digital signal processing (DSP) logic, which is tuned and constrained to meet the final product requirements. Although custom logic provides high-performance at low cost, it restricts the functional flexibility of the end product and comes with a high pre-silicon verification effort.

One way to balance the increasing engineering effort and costs with the growing need for flexibility is the adoption of a processing node next to the "Edge" of the system, thus aiming to the realization of a so-called **Software-Defined Radio** (SDR). As opposed to custom-logic signal processing units, an SDR provides the wanted flexibility at the cost of an initial non-recurrent engineering effort. In this case, the main challenge is finding the optimal system-partitioning, at early project stages, during concept development.

System partitioning entails HW/SW codesign to find the best tradeoff for the end-product business cases. In particular, it requires a design space exploration of different system architectures. Some of the metrics to be balanced are HW cost, power consumption, processing latency and throughput, as well as ease of support in the field. **Virtual Prototyping** (VP) provides an abstracted, flexible and fast way to explore tradeoffs between these metrics. A VP environment emulates a computing platform by using processor models in conjunction with models of peripherals and memories. Communication between system elements is achieved via **Transaction Level Modeling** (TLM).

Purpose

The aim of the **Master Thesis** proposed in this document is to develop a VP platform based around an open-source **RISC-V** processor and to identify and model the peripherals which are necessary to build a full-fledged SDR. As the SDR platform will be closely integrated with the rest of the existing system, the student will have the opportunity to understand the system-level interactions and design custom peripherals accordingly.

The VP platform will also model a memory subsystem with attached arbiter infrastructure. As the memory is shared between multiple top-level modules (one of which will be the SDR platform), arbitration delays on memory accesses, as well as bus-specific properties will be modeled to obtain a realistic performance estimation.

Finally, the student will run and profile the current software on the VP extensively. This also includes running a RISC-V core with custom DSP extensions in an RTL/TLM co-simulation environment.

Research Topics

Of particular interest for this Master work activity will be the identification of solutions in terms of HW/SW partitioning, SW algorithms and architecture, DSP processor requirements, logic and memory demands, clock rates and power consumption. This exploration will be supported by the analysis of the (Matlab) models describing the existing solution. Supported by a mentor, the student will have the opportunity to span over different disciplines, such as:

- Computer Architectures and Digital Signal Processing
- System Modeling & HW/SW Partitioning
- FW Development and Verification for Industrial Applications
- SoC Digital Logic Design and Verification

This Master work activity is part of a long-lasting collaborative program with the European Universities that the NFC Digital Modem team in NXP Gratkorn has initiated in year 2022. Each student is supported by a mentor who has the task to facilitate the activities, in line with the program objectives and deadlines.

As of day one, the student will be properly equipped, introduced and exposed to a fast-paced, multi-discipline and multi-cultural Digital HW development team, which holds responsibility from concept, design, and verification to silicon validation of the digital modem adopted in all NXP Secure NFC Controllers. The business line " Security & Connectivity", to which the team belongs, is currently the undiscussed market leader for Mobile Wallet, Secure Transactions and Identifications, as well as Wireless Charging solutions.

Student Profile

We are looking for students in the field of computer science, electrical engineering, software engineering or similar and with:

- A good knowledge of computer architectures and embedded systems
- Experience with embedded SW programming in C/C++ and understanding of OOP
- Ideally some first experience in SystemC and TLM
- An understanding of digital circuits design, HDL and verification techniques
- Academical background (if not also experience) in DSP theory and practice (e.g. in Matlab/Simulink)

Organizational Aspects

Start of activity:	as soon as possible;
End of Activity:	from six to nine months, after the start;
Workplace:	NXP Semiconductors Austria, Gratkorn; After ramp-up, we offer the option to work from home most of the time;
Paid thesis:	To be defined with NXP Austria recruiters;
Language:	English;
NDA:	Sign-off required to protect any NXP's business sensitive part touched by the master work.

Contact People and Supervisors

At NXP Semiconductors Austria:

- **Recruiter:** **Lisa Ziermann,** lisa.ziermann(at)nxp.com
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