Summary

ELECTRICAL MEASUREMENTS

BASICS ON MEASUREMENTS THEORY

When you're dealing with measurements on real systems it's of major importance to keep in mind that the results you obtain are not the actual values of measured variables but they are more or less close to them depending on many variables. Our goal on these lines is study how to formalize this concept and how to deal with various causes of uncertainties.

Conceptually a measure is not just a number as we are used to think, actually a measure it's a set defined as follows: $x_m = [\overline{x_m} - \delta_{xm}, \overline{x_m} + \delta_{xm}]$ where $\overline{x_m}$ is the central value of the measure and δ_{xm} is the uncertainty associated with it. The measurement instrument gives the value of $\overline{x_m}$ and the uncertainty evaluation is made by the measurer.

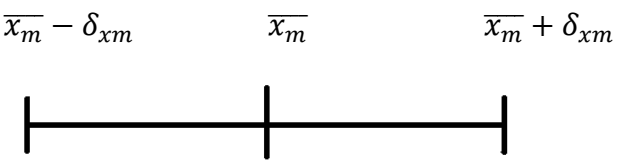


Figure 1-Measurement set

Sometimes the uncertainty is given relatively to the value of $\overline{x_m}$ and it's called relative uncertainty, while the other is called absolute uncertainty.

Assuming the measure has been performed correctly the uncertainty evaluation has to be done according to the type of measure. There exist two major sets of measurements:

- Direct measurements: In which the variable under investigation is directly measured by the instrument
- Indirect measurements: In which the variable under investigation is evaluated through multiple measurements on other variables and then put together mathematically.

To evaluate the uncertainty, it's necessary to fix a framework and then develop a theory according to it. There exist two major theories on uncertainty:

- Deterministic theory: It's based on the assumption that each measure has an uncertainty that contributes to the whole and theirs contributes are always positive; in practice the total uncertainty is the sum of the absolute values of the uncertainties of single measures.
- Probabilistic theory: It's based on the assumption that the uncertainty is a random variable with a proper probability density function and it must be chosen properly by the measurer.

On this tutorial just the deterministic theory will be explained and used. For whom are interested in probabilistic approach can read the section of this file related to it:

Useful link:
http://www.phy.uct.ac.za/sites/default/files/image_tool/images/281/people/buffler/Buffler%20CSIRO%20GUM%20talk.pdf

DIRECT MEASUREMENTS

In this case the uncertainty computation is just matter of read the user manual of the instrument, get the nominal uncertainty of the instrument and use it to evaluate what it's needed. Generally, there are many ways to write down on the user manual the uncertainty, the main ones used in electronics are listed below:

- Precision class: This method is used on analogic instruments and is based on the definition of class $Cl = \frac{|x_m - \bar{x}_m|}{FS} \cdot 100$ where FS is the full-scale value of the instrument. The manufacturer gives to the measurer the class index and so by solving for $|x_m - \bar{x}_m|$ the equation it's possible to obtain the uncertainty.
- Percentage on full scale: This method is generally used on digital instruments. The manufacturer gives a direct formula for the uncertainty, similar to this one: $\delta_{xm} = a \cdot FS + b \cdot x_m$ where the coefficients a and b changes with the chosen range.

INDIRECT MEASUREMENTS

In order to evaluate the uncertainty of an indirect measurement the measurer must know the mathematical model with which it's possible to evaluate the unknown and all the values of the uncertainties of single measurements. Once all these information are known this formula can be used:

$$\delta_y = \left|\frac{\partial y}{\partial x_1}\right| \cdot \delta_{x1} + \left|\frac{\partial y}{\partial x_2}\right| \cdot \delta_{x2} + \cdots + \left|\frac{\partial y}{\partial x_n}\right| \cdot \delta_{xn}$$

Where:

- y is the mathematical model which links all the measurements
- δ_{xi} is the relative uncertainty of the i-th measure

This formula can be decomposed in some recurring cases:

- $y = x1 \pm x2 \rightarrow \delta_y = \delta_{x1} + \delta_{x2}$
- $y = x1 \cdot x2 \rightarrow \delta_y = \delta_{x1} + \delta_{x2}$
- $y = \frac{x1}{x2} \rightarrow \delta_y = \delta_{x1} + \delta_{x2}$
- $y = x^n \rightarrow \delta_y = n \cdot \delta_{x1}$

If the mathematical model is more complex the general formula must be used.

All the instruments user manual can be found on led.polito.it, under Strumentazione section:

Useful link: http://led.polito.it/main_it/instrumentation.asp

BASIC INSTRUMENTATION

AMMETER

As the name suggest an ammeter is an instrument that can measure current values on a circuit. It's working principle (on analogic version) is quite easy and is based on the deflection of a rotating part due to a magnetic field proportional to the measured current. This interaction between the magnetic field and the current may be of two types:

- Moving coil: In this type the magnetic field is generated by a permanent magnet that interact with a coil in which is flowing the current under measure. Additionally, this coil is fixed with the needle that indicates on a scale the measurement; for this reason, is called moving coil instrument. If the current is an alternating one the needle just oscillates around an equilibrium position and no measure is available, for this reason this instrument is used to measure just direct currents.
- Fixed coil: Here instead of a permanent magnet there is just a soft iron piece fixed with the moving needle and the current under measure flows inside a fixed coil whose magnetic flux passes through the iron that is magnetized and generates a torque that moves the needle. In this case this torque is proportional to the square of the current, cancelling the problem of oscillations aroused with moving coil instruments. These instruments can be used to measure both alternating and direct currents.

Once the basic ammeter is defined it must be clear that it can't measure current higher than some milli-ampere, so it's a milli-ammeter. To measure higher current, it's possible to use to circuit depicted below:

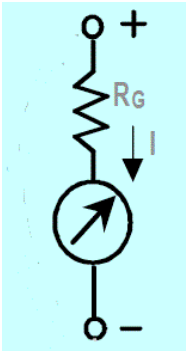


Figure 2-Ammeter diagram

The series resistance models the internal resistance of coil wires and the parallel one is used to drain a controlled current value to measure higher currents with a milli-ammeter. The internal resistance of ammeters is generally very low, in order to affect as less as possible the circuit.

To successfully measure a current on a circuit, the ammeter must be connected in a proper way. Since an electrical current derives from a solenoidal quantity it's path must be closed and to measure it the ammeter must be a part of this path. So, what it's needed is to open the circuit section in which I want to measure the current and put in between the ammeter in series with it. Be very careful with ammeter insertion because if it's connected in parallel with a component (i.e. a resistor), due to its low internal resistance, the current that flows in it may destroy the instrument.

VOLTMETER

A voltmeter is an instrument devoted to measure voltages in a circuit. The basic voltmeter is based on the ammeter making a sort of current-voltage conversion. To perform this conversion a series of high precision and high value resistor put in series with the ammeter and, through the Ohm's law it's possible to get the voltage value. The measurer does not have to know the internal resistance, read the current and apply the Ohm's law because the scale is already given in such a way that a certain needle deflection corresponds to the corresponding voltage.

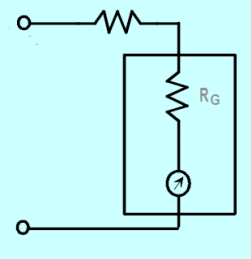


Figure 3-Voltmeter diagram

In order to measure a voltage, the two terminals of the voltmeter just have to be placed in the correct nodes of the circuit, so in parallel with it. A wrong insertion (series) does not cause any damage to the instrument due to its high resistance value, at least any current flow inside the circuit.

The correct connection for both the instruments is shown below:

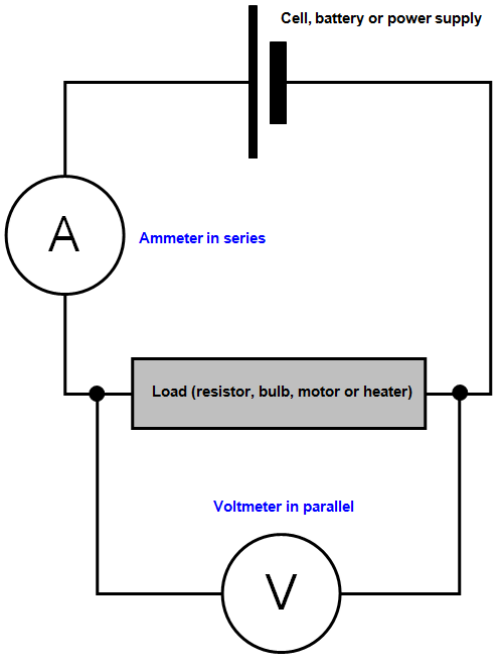


Figure 4-Correct connection for instrumentation

ACTIVE INSTRUMENTATION

DC POWER SUPPLY

Figure 5-DC power supply front panel

The DC power supply is devoted to supply power (voltage and current) to the electronic circuit. The power supply available in laboratory have the following characteristics:

- 2 independent channels are available
- Both channels have voltage and current limit regulation
- It's possible to let them work in independent or tracking mode
- Independent fixed voltage output

Let's analyze what these characteristics mean and to what them are useful to:

- Having 2 independent channels it's possible to supply the circuit with two different and unrelated voltages
- When prototyping it's possible to make mistake and damage component or instrumentation due to high currents. These supplies have current limitations with which is possible to set an upper limit (coherent with the maximum current fed to the circuit) to avoid any damage.
- Independent mode means that the two channels are regulated independently, while in tracking mode the Master channel (usually the 1) voltage knob, regulates also the voltage on channel two (Slave) to the same value. This is useful when a dual supply is needed (i.e. for operational amplifiers), connecting the outputs as shown in Figure 6.

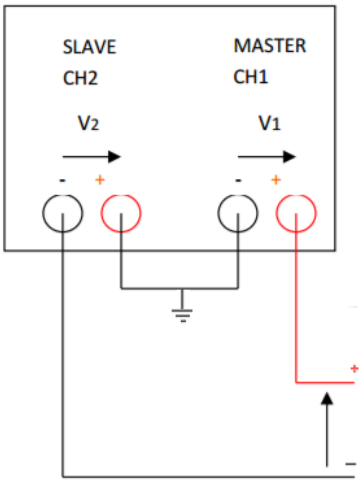


Figure 6-Dual supply connection

- In many applications may be useful to have a stable voltage to use as reference for some other component so the fixed voltage output may turn out to be the best solution, eventually reducing this voltage through a resistive voltage divider.

FUNCTION GENERATOR

When testing a circuit in many cases just a DC voltage is not enough, other waveforms such as sinusoidal, triangular or square, are needed. These time-variant voltages are generated by the function generator.

Figure 7-Function generator front panel

In order to successfully use this generator some parameters must be set correctly. The main ones are listed below:

- Frequency or period of the periodic waveform
- Amplitude (peak-to-peak, peak, upper and lower level)
- Offset (DC component)

To set the frequency rotate the knob or use the key pad to enter directly the number and then set the range (μHz to MHz). The same can be done to set the amplitude and the offset changing just the controlled variable (frequency to amplitude or offset).

Be careful to the maximum amplitude the generator can handle because the most common error in these cases is to not consider that this voltage value is the sum of amplitude and offset: $\hat{V} + V_{off} \leq V_{max}$.

Other more advanced regulations one can make on the function generator are:

- Symmetry adjustments
- Duty cycle regulation
- Output impedance value regulation

About the symmetry the most clarifying example may be the triangular wave:

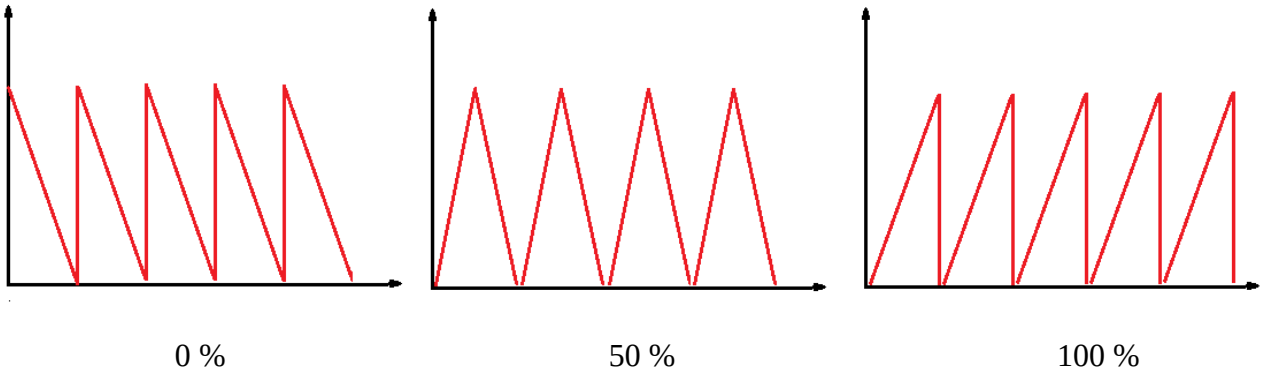


Figure 8-Triangle signal symmetry

The duty cycle regulation is available just for square wave signal and allows to change the time for which the signal is at high level for each period, that is exactly the duty cycle definition: $\delta = \frac{T_{on}}{T}$
The output impedance value regulation is not a proper action on the output impedance of the function generator but, depending on what is the selected choice it automatically correct the output voltage. On these function generators there are two possibilities: 50 Ω or high impedance load.

- 50 Ω: Selecting this value you are telling the function generator that the line has a characteristic impedance of 50 Ω between the generator and the load. If you want to have, for example, 2 V on the load, it automatically doubles the actual voltage output to cancel the effect of the voltage divider made by the line and the load.
- High impedance load: Selecting this value the actual voltage on the output is the selected one, because the line is supposed to have much lower impedance than the load, so voltage drop on it are negligible.

Finally, sometimes two signals may be required to test completely a circuit and they must be synchronized (relative phase must be zero). To achieve that, once the two signals are available on the outputs, the button SYNC must be pressed.

OSCILLOSCOPE

The oscilloscope is used to visualize on a screen a voltage with respect to time. There are nowadays two different type of oscilloscopes: analogic and digital. An analogic oscilloscope, in its simplest form, read the signals on inputs and display them on a CRT screen, so through an electron gun and a phosphorescent screen. The electron rays are bent by magnetic fields that are proportional to input signal. A digital oscilloscope has usually a LCD screen in which the signal trace is generated by a processor accordingly to the preferences the measurer have selected. Here we focus just on digital oscilloscopes (also called DSO) that are becoming pervasive on electronic laboratories. This instrument has a lot of different knobs and buttons to get all the information from the signal. In the figure below is represented the front panel of the one we have in the laboratories and the most important regulators are highlighted with different colors:

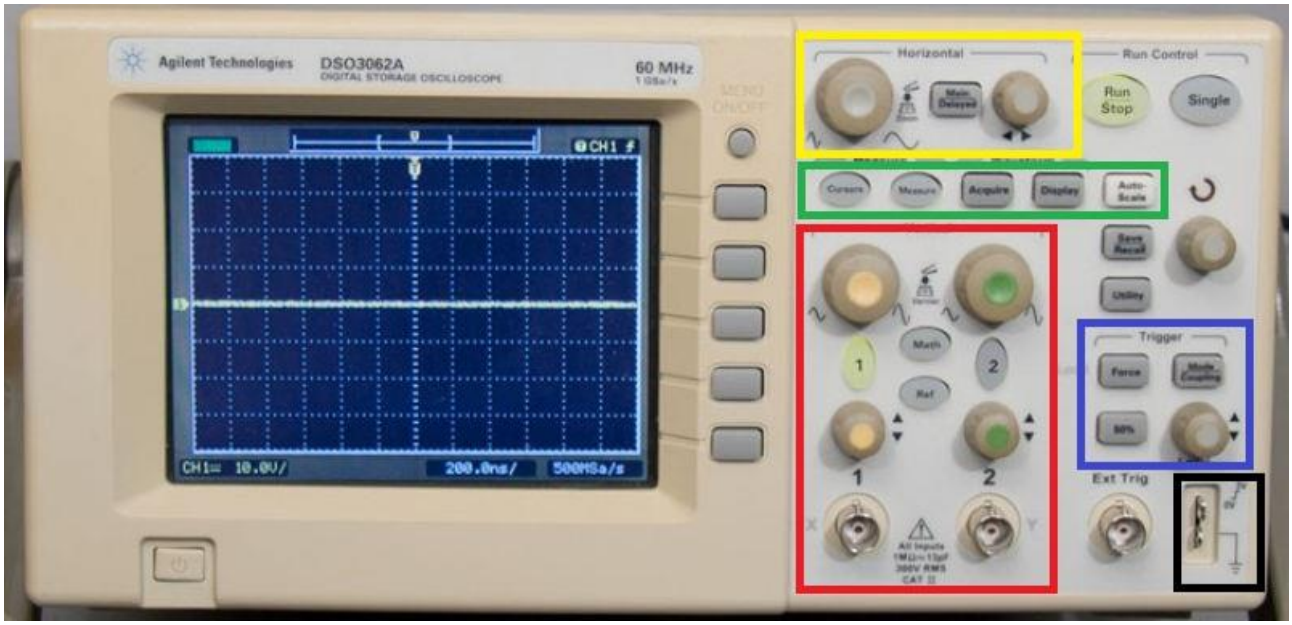


Figure 9-Oscilloscope front panel

SCREEN

The screen, in normal operations, gives to the measurer three information:

- The waveform on a 6x4 matrix, where each division is divided in 5 sub-divisions to perform more accurate measurements
- The amplitude constant which tells how many volts are represented by one division on the vertical axis. On the example this number is on the bottom left of the screen and tells that each division corresponds to 10 V.
- The time constant that works in the same way as the amplitude one but is related to the horizontal axis and represents how much time a single division lasts.

Other important information are the arrows on the top and left center which represent the zero value, for both time and amplitude, from which the signal is drawn on the screen.

RED BOX (Amplitude regulation)

This region is devoted to the input connections and the preferences regulations for both channels.

- Starting from the bottom there are the two input BNCs where the probes are connected
- Then, going up, there are the two zero-regulation knobs, with which is possible to move the zero position of the respective signal. In other words, by rotating them is possible to move up and down the signal trace on the screen.
- The buttons with numbers on them allows to select which of the two signal are visualized on the screen. The green highlighted one is the chosen channel and it's possible to visualize both, in this case they will be both highlighted.
- The bigger knobs are the ones with which it's possible to change the amplitude constant. So by turning it the displayed signal will be shown bigger or smaller in y-direction.

Finally, there is a Math option button, that allows to make some basic math operations on the signals coming from the two inputs. This may turn out to be useful to get non-measured signal traces, for example through mesh equations.

YELLOW BOX (Time base regulation)

In this part of the front panel just focus on the two knobs:

- The bigger one is used to change the time base of the oscilloscope so, by turning it, it's possible to stretch/squeeze the trace to fit it in the screen. Usually, when the signal is periodic, one or two periods of the signal should be visualized.
- The other one allows to pan on the horizontal axis the trace. So by turning it the signal trace will be panned on time axis.

GREEN BOX (Other functions)

Here there are 3 buttons of our interest that are listed and explained below:

- The first on the left, named cursors, allows to put horizontal and vertical cursors on the screen which are used to make measurements by putting them in our interest points. To move these cursors what is needed is just to rotate the knob on the right, the one under the circular arrow.

- The second button, named measure, allows to get a lot of information from the signal automatically, both on time domain and amplitude domain. Once this mode is selected, the measurer should choose the channel on which he wants to make measures and select if the measures are on time or voltage. Some of the most used measures are listed below:
    - Time domain
        - Frequecy
        - Period
        - Rise time
        - Fall time
        - Duty cycle

- Voltage domain
  - Vpp (peak to peak voltage)
  - Vavg (average voltage)
  - Vrms (RMS value of the voltage)

This mode is much more precise than the previous one so, if the measure we want to make is available on measure mode, use it instead of cursor one

- The button on the right (the final one), named auto-set, is something that allows to solve automatically some problems that may arise during measurements, such as running trace, no trace on the screen, etc. This function set automatically the oscilloscope parameters to have a clear trace on the screen that is a good starting point to make fine adjustments and display it as we want. Be careful that auto-set is something that may help us but, once used, look to what are the chosen parameters, and correct them if wrong.

BLUE BOX (Trigger)

In this box are enclosed the trigger regulations. In an oscilloscope, the trigger is a signal that starts the visualization of the trace on the screen. As one can imagine if the signal and the trigger are not synchronous, the trace will have a different starting point each time it is displayed and this phenomenon is the so called "running trace", because the oscilloscope can't "stop" the trace at one precise point. The trigger signal may come from EXT trigger BNC input (EXT mode) or may be generated starting from the input signals on CH1 and CH2 (this is what is usually done). In order to properly set the trigger three parameters have to be taken into account:

- Source: Choose among EXT, CH1, CH2, as explained before
- Slope: The trigger signal is generated on a given signal slope, positive or negative, depending on the measurer necessities.
- Level: Is the amplitude of the signal on EXT, CH1, CH2 on which the signal is generated.

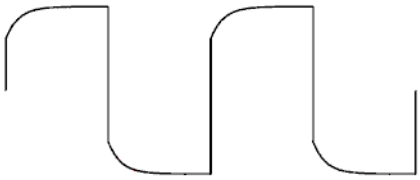
The most common errors may come from a wrong choice of the source and level. To change these parameters, look at the little knob and to the button just above it. The button allows to open the trigger menu, where it's possible to choose the slope and the source while, the knob, allows to change the level which is represented on the screen though a horizontal dotted line that move up and down while turning the level knob. Clearly this line must cross the displayed signal at least in one point.

BLACK BOX (Probe adjustment)

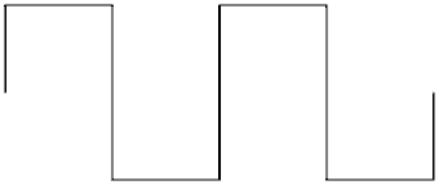
Here there are the contacts of a square wave generator with well-known amplitude and frequency that is used to calibrate the probe before using it. The probe, differently from a normal coaxial cable has inside a circuit that, once properly calibrated by the measurer, allows to eliminate or at least reduce the effect of frequency on the measure circuit. When making measurements on a circuit some other components are inserted on it and their frequency behavior influences the measurement. So if a probe is used the first thing to do is to connect the BNC to and input of the oscilloscope and then "measure" with it the square wave signal across these two contacts.

Mainly three things may happen:

- Under-compensation



- Correct-compensation



- Over-compensation

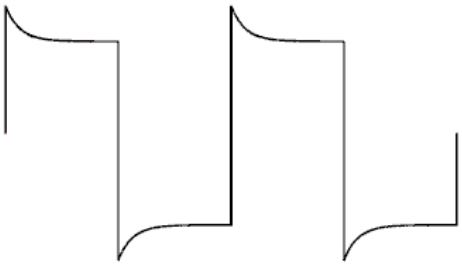


Figure 10-Probe compensation

In order make the compensation just rotate the little screw inside the probe that acts on a variable capacitor, which can compensate frequency effects.

Figure 11-Oscilloscope probe

OTHER FEATURES

Once the basic functions of an oscilloscope are clear on mind, some other features must be explained in order to successfully use the instrument.

- X-Y visualization: In this way, it's possible to use CH1 as "time-base" and CH2 as amplitude. This mode turns out to be useful when testing input-output characteristics of circuits, by connecting the input to CH1 and the output to CH2. A typical example is the visualization of the hysteresis cycle of a Schmitt's trigger.
- Input impedance: The input impedance of an oscilloscope is composed by a 1 MΩ resistor with a 40 pF capacitor in parallel. This may bring to unexpected errors on visualization and must be considered when the equivalent resistance is near 1 MΩ (may bring to voltage divider effects). The effect of the capacitor may be reduced through probe compensation.
- Limited bandwidth: Each measurement instrument has a limited bandwidth, which means that the signal above this frequency limit are attenuated as much as higher the frequency. Actually, the input signal fundamental frequency will not exceed this limit but some harmonics may easily go beyond it. An example of such a signal is the square wave that, even if has low frequency, higher harmonics are inside it to allows steep rising and falling edges so, if the displayed signal is more similar to a trapezoid, it does not mean that the actual signal is a trapezoid, but it's just an error introduced by the oscilloscope due to limited bandwidth. To compute the error on rising and falling edge introduced by the oscilloscope this formula can be used: $\Delta t = \frac{0.35}{Bandwidth}$, which is usually so low to be easily neglected.

SUMMARY

Down below there is a summary of most common mistake a beginner may make when using this instrument. This is intended to be a ready to use guide to correct possible misbehaviors of the oscilloscope:

- No signal on the screen:
  - Make sure that the correct channel is selected on the red box
  - Make sure that the zero-line is displayed on the screen. The signal may be outside the screen on vertical direction.
  - Make sure that Run-Stop button is green-highlighted.

- The signal is in free-running on the screen:
  - Wrong trigger source. Select the correct channel.
  - Wrong trigger level. Remember that, when that when displaying two trace on the screen the trigger level must be set according to the trigger source.
- The signal amplitude is different from the expected (before thinking that the circuit is wrong):
  - The probe amplifier selector (x1 x10 x100) is set on the wrong position
  - …
- The measures made with the Measure tool are not exact
  - Make sure that the measure is made on the correct channel
  - Since the measure is made on the acquired samples, make sure that enough samples have been acquired (1-2 period of the signal).
  - Try with another equivalent instrument (voltmeter,…) to check whether the measure made by the oscilloscope is right or not.

Useful link: https://learn.sparkfun.com/tutorials/how-to-use-an-oscilloscope/all

BREADBOARD

The breadboard is the place where all the electronic circuits are built for prototyping purposes.

Useful link: https://learn.sparkfun.com/tutorials/how-to-use-a-breadboard

HOW TO USE IT PROPERLY?

Due to its physical structure the breadboard is subjected to many phenomena that must be considered to realize a proper circuit on it. The main issues are listed below:

- Coupling capacitance: Due to the proximity of the conductive lines inside the breadboard there is a capacitance (around 20 pF) between them. This may lead to an unwanted signal coupling that does not make the circuit work properly. Since the capacitive impedance is inversely proportional to the signal's frequency a breadboard can handle frequencies of 5-10 MHz.
- Contacts resistance: Due to the kind of contact on the breadboard, a very low resistance contact is not possible. The usual resistance value is around 0.1-0.5 Ω.

- Voltage divider effects: Due to parasitic elements on the breadboard some counter-effects may be seen on a working circuit. One of them is a voltage divider effect that may be due to both resistance and capacitance. When using low value resistors (shunt) or low value capacitors (for example as high frequency component filters) the voltage on them is split on the actual component and on the parasitic one.
- Maximum ratings: The board cannot handle high power because of the nature of contacts and strips. Generally, the rated power is around 5 W.

These facts must be considered when prototyping the circuit to know whether the circuit can be tested on a breadboard or not (for example if it works ad very high frequency).

CLEAN ASSEMBLY

Another important issue is a clean assembly of the components on the breadboard because a messy one may lead to misbehaviors at high frequencies and to an unnecessary effort when troubleshooting it. The main rules of thumb are listed here:

- Mount the components in horizontal or vertical orientation.
- Cut the unnecessary wire on components, making them being as near as possible to the board.
- Use less wires as possible.
- Use as short wires as possible.
- Use dedicated power lines to deliver the supply voltage.

BREADBOARD SIMULATOR

Useful link: http://fritzing.org/home/

TREE PHASE SYSTEMS

WHAT'S A THREE PHASE SYSTEM?

PHASORS

Three-phase systems are commonly used in generation, transmission and distribution of electric power. Power in a three-phase system is constant rather than pulsating and three-phase motors start and run much better than single-phase motors.

The phase variable $x_a(t)$, $x_b(t)$ and $x_c(t)$ are as follows:

$$x_A(t) = X_A \cos(\omega t)$$
$$x_B(t) = X_B \cos(\omega t + 120°)$$
$$x_C(t) = X_C \cos(\omega t - 120°)$$

Where x is a generic electric variable (voltage or current). Translating the trigonometric functions into complex exponential we derive the phasor form:

$$x_A(t) = X_A e^{j\omega t}$$
$$x_B(t) = X_B X_A e^{j(\omega t + 120°)}$$
$$x_C(t) = X_C X_A e^{j(\omega t - 120°)}$$

This form is very useful because allows to manage 3 time varying functions as rotating vectors (phasors).

If $X_A = X_B = X_C$ the system is balanced. In order to have a balanced three phase system the voltages must be equal and load impedances must be equal. The vector representation is shown here:

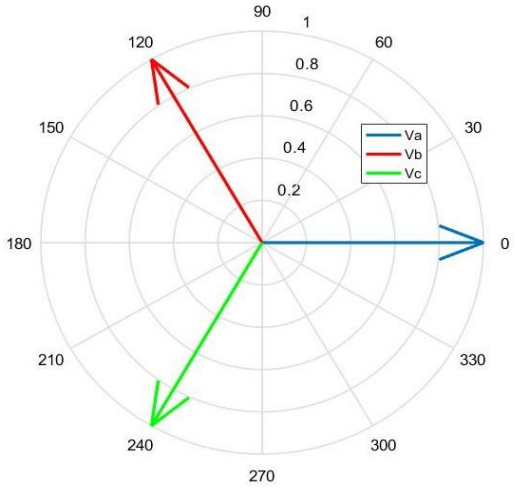


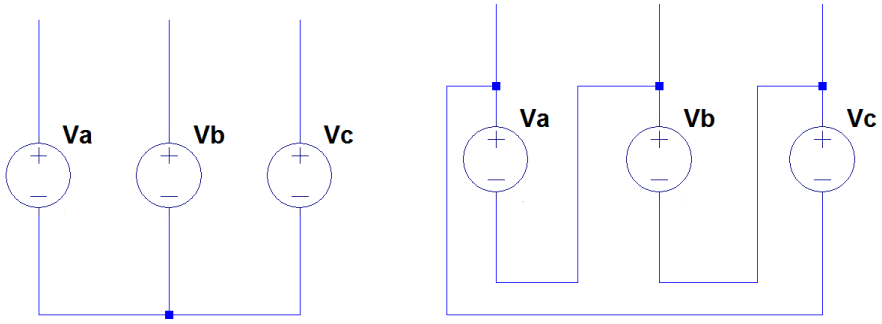
Figure 12-Phasor's diagram

Look here to learn more about phase rotation and the relation with rotating machines:

Useful link: https://www.allaboutcircuits.com/textbook/alternating-current/chpt-10/phase-rotation/

DELTA-STAR CONNECTION

Typically, two connections are used in 3 phase systems in order to connect power supplies and load impedances: delta and star connection.



Star Delta

Figure 13-Delta-Star connection schematic

The kind of connection depends strongly on technological constraints that may arise when designing something i.e. voltage level, current recirculation, ecc…
In these circuits we may find 2 set of variables:

- Line variables
- Phase variables

whose definition depends on the considered variable:

- Phase voltage: The voltage across an impedance in star connection or, equivalently, the voltage across the supply positive output and ground.
- Line voltage: The voltage across an impedance in delta connection or, equivalently, the voltage across two wires connected to the positive supply output.
- Phase current: The current passing through an impedance.
- Line current: The sum of two phase currents in delta connections.

The following relations holds among these variables

Star connection

$$(I_{eff})_L = (I_{eff})_P$$

$$(V_{eff})_L = \sqrt{3}\,(V_{eff})_P$$

Delta connection

$$(I_{eff})_L = \sqrt{3}\,(I_{eff})_P$$

$$(V_{eff})_L = (V_{eff})_P$$

Look here to have more information and some examples:

Useful link: https://www.allaboutcircuits.com/textbook/alternating-current/chpt-10/three-phase-y-delta-configurations/

EQUIVALENT CIRCUIT

Every 3 phase system can be represented by an equivalent circuit, made in this way:

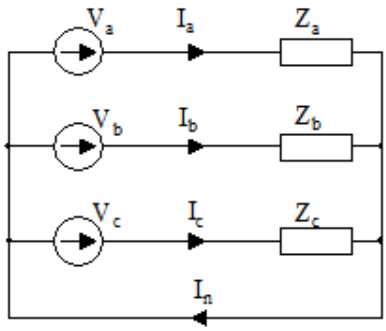


Figure 14-A generic 3-phase system

This is a star connection circuit but it's also valid for delta connections through the well-known conversion formulae.

SOLVING A THREE PHASE CIRCUIT

Three important things must be considered when solving AC circuits:

- Variables are phasors (complex numbers) so use the proper formulas to treat them. The most common error is to sum and subtract vector by summing or subtracting its magnitude that is wrong; sum component by component, then if required get the resultant magnitude.
- Millmann's theorem: Due to the particular topology (2 nodes) of the equivalent circuit the Millmann's theorem is the most effective.
- If possible, use Boucherot's theorem (power conservation) to reduce at most the calculations with complex numbers.

For a balanced three phase system, by applying the Millmann's theorem to the circuit, results that the voltage across the neutral wire is 0, so the three-phase system reduces to 3 single phase systems that behaves equally in terms of phasors. In this way, we derive the so called One-Line diagram, much more simple to solve.

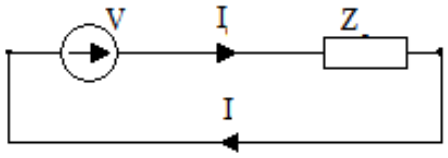


Figure 15-Single phase equivalent circuit

TWO SIMPLE EXAMPLES

1)

Two AC currents are summed in a node, what is the total current? $I_1 = 1 + j5\ A \quad I_2 = 10 < 12°\ A$

Do not sum the magnitudes, but the complex components:

$I_2 = 10 < 12° = 10\cos(12) + j10\sin(12) = 9.78 + j2.07$ A

$I_{tot} = Re(I_1) + Re(I_2) + j(Im(I_1) + Im(I_2) = 1 + 9.78 + j(5 + 2.07) = 10.78 + j7.07\ A$

2)

Consider the three phase equivalent circuit above where now:

$|V_a| = |V_b| = |V_c| = 100\ V$

$< V_a = 0°$

$Z_L = 5 + j5\ \Omega = \sqrt{50} < 45°$

Find the current on each phase, expressing it in phasor form (complex exponential).

Through the one-line diagram:

$I_a = \frac{V_a}{Z_L} = \frac{100}{\sqrt{50}<45°} = 7.07 < -45°\ A = 7.07\ e^{j(\omega t - 45°)}$

And through the time shift of 120° electrical degrees

$I_b = 7.07\ e^{j(\omega t - 45° + 120°)}$

$I_c = 7.07\ e^{j(\omega t - 45° - 120°)}$

The amplitude is equal because of the balanced system.

POWER IN THREE PHASE SYSTEMS

As in a classical AC circuit analysis three kind powers are involved:

- Active power [P]
- Reactive power [Q]
- Complex power [S]

In the balanced systems, the average power consumed by each load branch is the same and given by

$$\widetilde{P} = V_{eff} I_{eff} \cos\phi$$

where V_{eff} is the effective value of the phase voltage, I_{eff} is the effective value of the phase current and ϕ is the angle of the load impedance. The total average power consumed by the load is the sum of those consumed by each branch, hence, we have

$$P = 3\widetilde{P} = 3V_{eff} I_{eff} \cos\phi$$

In the balanced star systems, the phase current has the same amplitude as the line current $I_{eff} = (I_{eff})_L$, whereas the line voltage has the effective value $(V_{eff})_L$ which is $\sqrt{3}$ times greater than the effective value of the phase voltage, $(V_{eff})_L = \sqrt{3} V_{eff}$. Hence we obtain

$$P = 3\frac{(V_{eff})_L}{\sqrt{3}}(I_{eff})_L \cos\phi = \sqrt{3}(V_{eff})_L (I_{eff})_L \cos\phi$$

Similarly, we derive

$Q = \sqrt{3}(V_{eff})_L (I_{eff})_L \sin\phi$.

The term S, complex power, is defined as follows:

$S = \sqrt{3}\, V_{eff} I_{eff}^*$ where I_{eff}^* is the complex conjugate of the effective current.

Developing this product what comes out is:

$S = P + jQ$

A simple exercise:

Using the same daa of the previous exercise, find the generated power by the generator Va.

$$S_1 = \sqrt{3}\, V_1 I_1^* = \sqrt{3}\ 100 < 0 \cdot \frac{100}{\sqrt{50}} < (-45° + 90°) = \sqrt{3}\ \frac{10000}{\sqrt{50}} < 45° = 490\ W + j490\ Var$$

$$|S_1| = \sqrt{490^2 + 490^2} = 693\ VA$$

Here there is another explanation of these concepts with some examples:

Useful link: https://www.allaboutcircuits.com/textbook/alternating-current/chpt-11/power-resistive-reactive-ac-circuits/

If the Reader wants to go deeper in these concepts, below there are some suggested links (Not mandatory to attend successfully the future courses)

Basic DC circuit theory

http://www.allaboutcircuits.com/video-lectures/basic-requirements-for-current/

Basic AC circuit theory

http://www.allaboutcircuits.com/video-lectures/generation-of-alternating-voltage/

Three phase systems

http://doctord.dyndns.org/Courses/Textbooks/Chapman/Lecture%2003%20-%203phase.pdf

http://my.ece.msstate.edu/faculty/donohoe/ece3614three_phase_power.pdf

ELECTRIC DRIVES

WHAT IS AN ELECTRIC DRIVE?

DEFINITION OF ELECTRIC DRIVE

By definition, an electric drive is an arrangement of electrical motors AND controls that allows to control the motor, fulfilling the required specification for the given process.

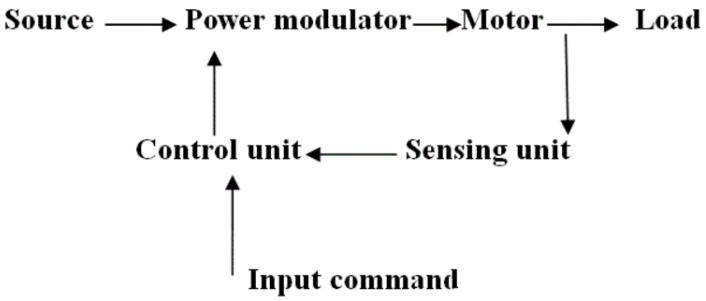


Figure 16-Generic structure of an electric drive

- Source: Power supply
- Power modulator: Electronic converter
- Motor: Electric motor
  - DC Motor
  - Synchronous motor
  - Asynchronous motor
  - Stepper motor
- Sensing unit: Various sensors (i.e. encoder for position and speed)
- Control unit: Computes set-points given sensed variables
- Input command: Speed and torque reference.

TYPES OF ELECTRIC DRIVES

The controlled variables are torque and speed. Putting them as variables of a Cartesian plane it's possible to define the so called working quadrants

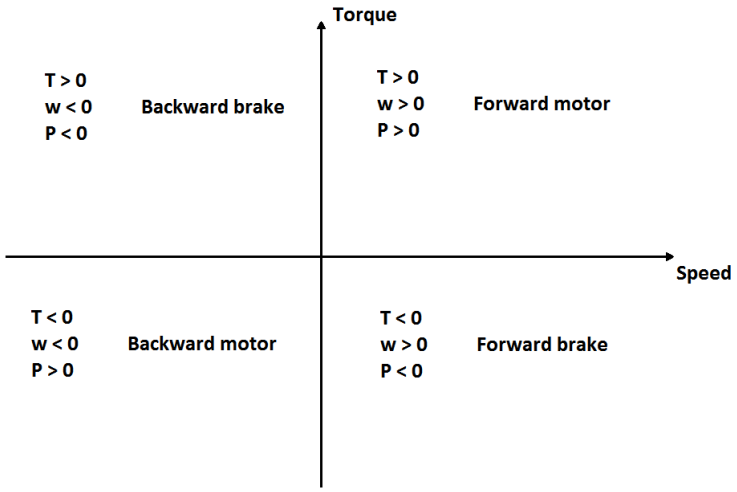


Figure 17-Speed/Torque plane

The main subdivision of electrical drives is on this working quadrants.

EXAMPLE

- 1 quadrant drive is just able to work as motor or brake in just one direction
- 2 quadrants drive is able to run as motor or brake in just one direction
- 4 quadrants drive is able to run as motor or brake in both directions

Another classification is made on the dynamic behavior of the drive:

- Spindle applications
  - Constant torque
  - High bandwidth to respond quickly to load variations
  - Example: Lathe, milling machines
- Axle applications
  - No load torque, just inertial
  - High bandwidth on speed control
  - Precise positioning
  - Example: Cartesian robots, ecc…

Other classification may be made on the type of motor and/or control used

- Motor: Same subdivision as before
- Control
  - AC
    - Scalar control
    - Field oriented control
    - Other control strategies
  - DC
    - Field control
    - Armature voltage

Look here for a more detailed classification:

Useful link: http://www.electrical4u.com/classification-of-electrical-drives/

SIMPLIFIED THERMAL MODEL OF A MOTOR

When designing, or using an electric drive it is mandatory to consider thermal characteristics of the motor, to avoid unwanted damages. The simplest model one can use is the one described here:

Useful link: https://www.electrical4u.com/thermal-model-of-motor/

GENERAL CONTROL STRUCTURE

To control the behavior of an electric drive there are thus 2 variables to consider, the torque (T) and the rotational speed (n) so, putting just a set-point as input for the electronic converter is not enough. The two control channels may be independent or coupled, depending on the working point of the motor.

The two main types of working methods for an electric motor are listed below and represented in Figure 3.

- Constant torque: It's possible to set a reference torque (below the rated one T*) and set the reference speed (below a limit value denoted as n*), within a range defined by a rectangle with side length (T*,n*).
- Constant power: It' possible to set the reference torque and the reference speed within a range upper-bounded by a hyperbole (with constant power the torque is inversely proportional to the speed). Used when need to go beyond n*.

To achieve the goal of controlling independently the two channels it's possible to use magnetic characteristics of electrical machines, combined with proper control strategies, namely:

- Field current and armature voltage control for DC motor
- D-Q axis current control for AC motor

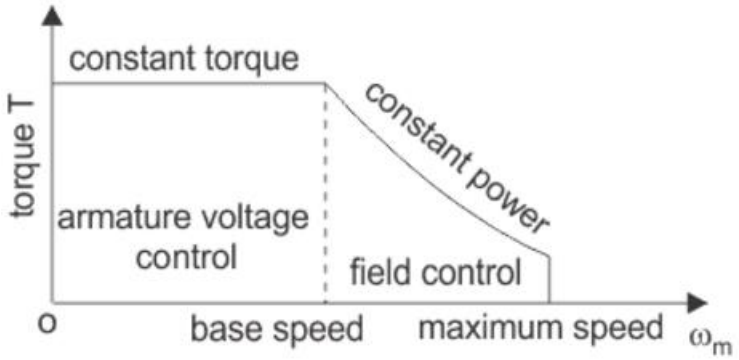


Figure 18-Constant power/Constant torque regulation

A nested loop topology is generally used because in this way it's possible to preserve the motor from dangerous high currents.

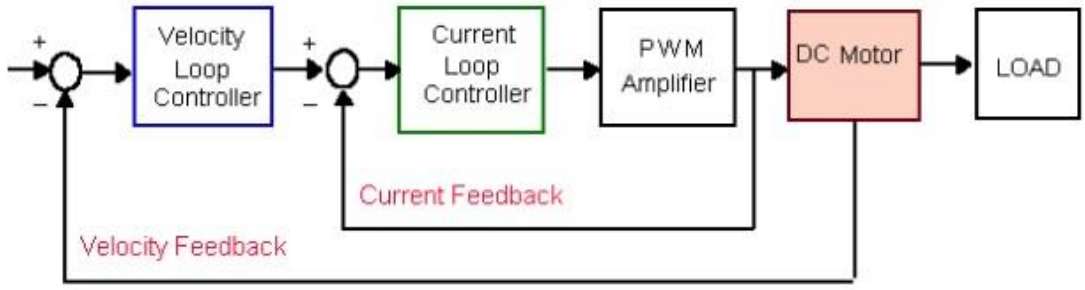


Figure 19-Nested loops control structure

Since the two loops need to maintain the set point, even in presence of disturbances coming from the external environment, a feedback loop controller must be used. Even though more sophisticated controllers must be used (LQR, H-infinity, ecc…), here is presented a configuration with a PI controller for each loop. The method to set the controller parameters is not presented here, where there is just a behavioral description of the influence they have on the controlled system. The transfer function of the controller is: $G_{PI}(s) = K_P + \frac{K_I}{s}$ and the effects of the gains are:

- Kp: This value is inserted as a pure gain in the direct path of the feedback control system and allows to make the electric drive faster to set-point variations and allows to reach a lower steady state error if no integral action is present. The drawback of increasing this value is that the system becomes more and more less stable.
- Ki: This value is the weight assigned to past error values. A higher value allows to better recover an error to reach the steady state condition in case of, for example, disturbances. If it is too high even a small error is amplified and the controller will overreact.

Here something more on speed/torque control:

Useful link: https://www.electrical4u.com/control-of-electrical-drives/

If the Reader wants to go deeper in these concepts, below there are some suggested links (Not mandatory to attend successfully the future courses)

Basics on DC motors characteristics:

http://lancet.mit.edu/motors/motors3.html

Something on stepper motors:

https://www.electrical4u.com/stepper-motor-drive/

A complete course on electric drives and related power electronic section (both AC and DC)

https://www.youtube.com/playlist?list=PLXppKURuY3ClrI9hDXqrE6gfkGKhEhpHX

ELECTRONIC COMPONENTS AND CIRCUIT ANALYSIS:

FUNDAMENTAL PASSIVE ELECTRONIC COMPONENTS (R,L,C):

PASSIVE COMPONENTS INTRO / BEHAVIOR AND POWER:

RESISTOR:

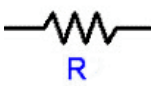


Figure 1 Resistor symbol

The relationship between the current through a conductor with resistance and the voltage across the same conductor is described by **Ohm's law**:

$$V = IR$$

where V is the voltage across the conductor, I is the current through the conductor, and R is the resistance of the conductor. The power dissipated by the resistor is equal to the voltage multiplied by the current:

$$P = IV$$

If I is measured in amps and V in volts, then the power P is in watts. By plugging in different forms of $V=IR$, we can rewrite $P=IV$ as:

$$P = I^2R$$

or

$$P = \frac{V^2}{R}.$$

CAPACITOR:

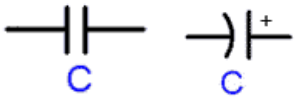


Figura 2 Capacitor symbol

The capacitor on the right is *polarized*. The potential on the straight side (with the plus sign) should always be higher than the potential on the curved side.

Notice that the capacitor on the far right is polarized; the negative terminal is marked on the can with white negative signs. The polarization is also indicated by the length of the leads: the short lead is negative, the long lead is positive. A capacitor is a device that stores electric charges. The current through a capacitor can be changed instantly, but it takes time to change the voltage across a capacitor**.** The unit of measurement for the capacitance of a capacitor is the *farad*, which is equal to 1 coulomb per volt.
The charge(q), voltage (v), and capacitance(C) of a capacitor are related as follows:

$$q(t) = Cv(t)$$

where q(t) and v(t) are the values for charge and voltage, expressed as a function of time.

Differentiating both sides with respect to time gives:

$$i(t) = C\frac{dv}{dt}$$

Rearranging and then integrating with respect to time give:

$$v(t') = \frac{1}{C}\int_{t_0}^{t'} i(t)dt + v(t_0)$$

If we assume that the charge, voltage, and current of the capacitor are zero at $t_0 = -\infty$, our equation reduces to:

$$v(t') = \frac{1}{C}\int_{-\infty}^{t'} i(t)dt$$

The energy stored in a capacitor (in joules) is given by the equation:

$$w_C(t) = \frac{1}{2}Cv^2$$

INDUCTOR:

Figure 3 Inductor symbol

An inductor stores energy in the form of a magnetic field, usually by means of a coil of wire. An inductor resists change in the current flowing through it. The voltage across an inductor can be changed instantly, but an inductor will resist a change in current. Unless we are tuning an oscillator or something, we generally don't purposefully add inductors to mechatronics circuits. However, any device with coils, such as motors or transformers, add inductance to a circuit. The relationship between the voltage across the inductor is linearly related by a factor *L*, the inductance, to the time

rate of change of the current through the inductor. The unit for inductance is the *henry*, and is equal to a volt-second per ampere.
The relationship between the voltage and the current is as follows:

$$v(t) = L\frac{di}{dt}$$

If we multiply both sides by *dt*, we get:

$$di = \frac{1}{L}vdt$$

Integrating both sides from t_0 to t' gives:

$$i(t') - i(t_0) = \frac{1}{L}\int_{t_0}^{t'} vdt$$

which is equal to:

$$i(t') = \frac{1}{L}\int_{t_0}^{t'} vdt + i(t_0)$$

assuming that the voltage, current and energy of the inductor are all zero at $t = -\infty$ reduces the equation to

$$i(t') = \frac{1}{L}\int_{-\infty}^{t'} vdt$$

The energy stored in the inductor is given by:

$$w_L(t) = \frac{1}{2}Li^2$$

ELEMENT IN SERIES AND PARALLEL

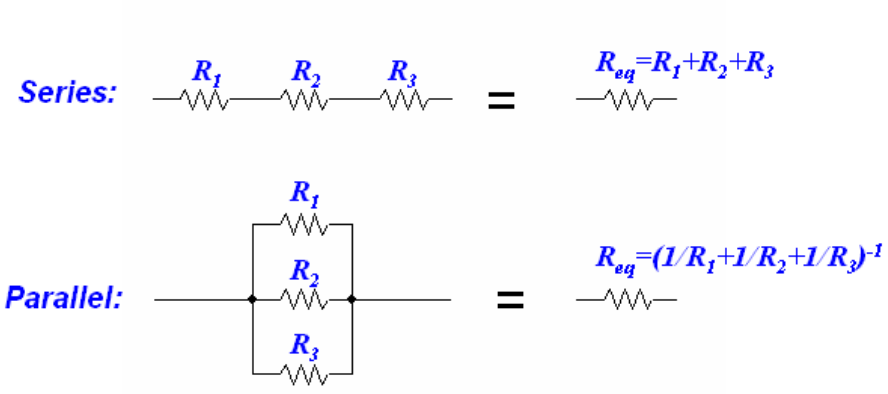


Figure 4 Series and parallel elements

For further information check webpage:

Useful link:
http://hades.mech.northwestern.edu/index.php/Resistors_(Ohm's_Law),_Capacitors,_and_Inductors

CHARGE/DISCHARGE OF A CAPACITOR:

When a battery is connected to a series resistor and capacitor, the initial current is high as the battery transports charge from one plate of the capacitor to the other. The charging current asymptotically approaches zero as the capacitor becomes charged up to the battery voltage. Charging the capacitor stores energy in the electric field between the capacitor plates. The rate of charging is typically described in terms of a time constant RC.

Two Elements in Series and Parallel

	Resistor	Capacitor	Inductor
Series	$R_{eq} = R_1 + R_2$	$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$	$L_{eq} = L_1 + L_2$
Parallel	$R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$	$C_{eq} = C_1 + C_2$	$L_{eq} = \frac{L_1 L_2}{L_1 + L_2}$

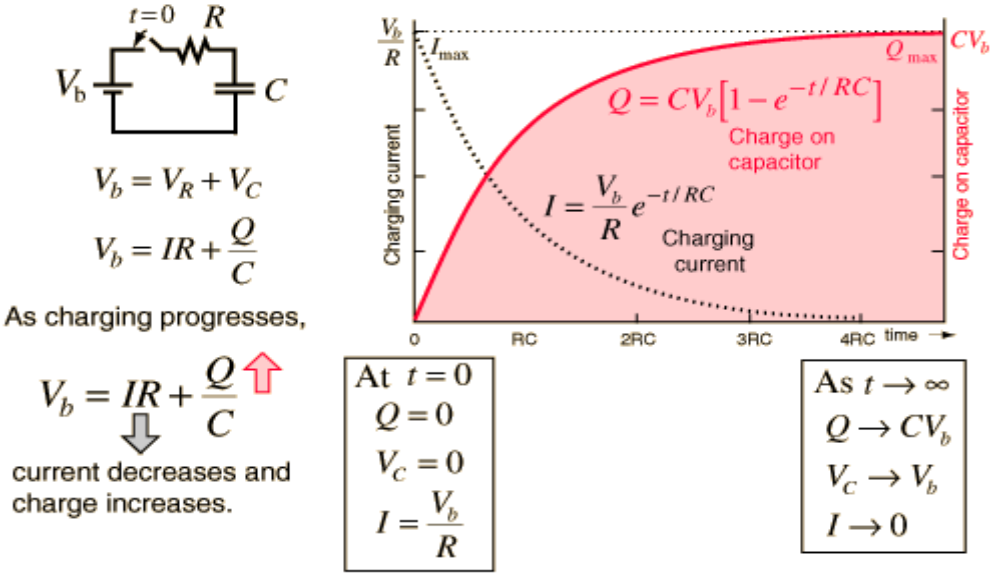


Figure 5 Charge and discharge of a capacitor

For useful notions and examples of the dynamic behavior of the capacitor check this web page:

Useful link: http://hyperphysics.phy-astr.gsu.edu/hbase/electric/capchg.html

EXAMPLES

CHARGING AND DISCHARGING A CAPACITOR (EXERCISE):

Useful link: http://munro.humber.ca/~lloyd/tech101/Capacitor%20Exercise.pdf

CHARGE/DISCHARGE OF AN INDUCTOR:

When a battery is connected to a series resistor and inductor, the inductor resists the change in current and the current therefore builds up slowly. Acting in accordance with Faraday's law and Lenz's law, the amount of impedance to the buildup of current is proportional to the rate of change of the current. That is, the faster you try to make it change, the more it resists. The current builds up toward the value it would have with the resistor alone because once the current is no longer changing, the inductor offers no impedance. The rate of this buildup is characterized by the time constant L/R . Establishing a current in an inductor stores energy in the magnetic field formed by the coils of the inductor.

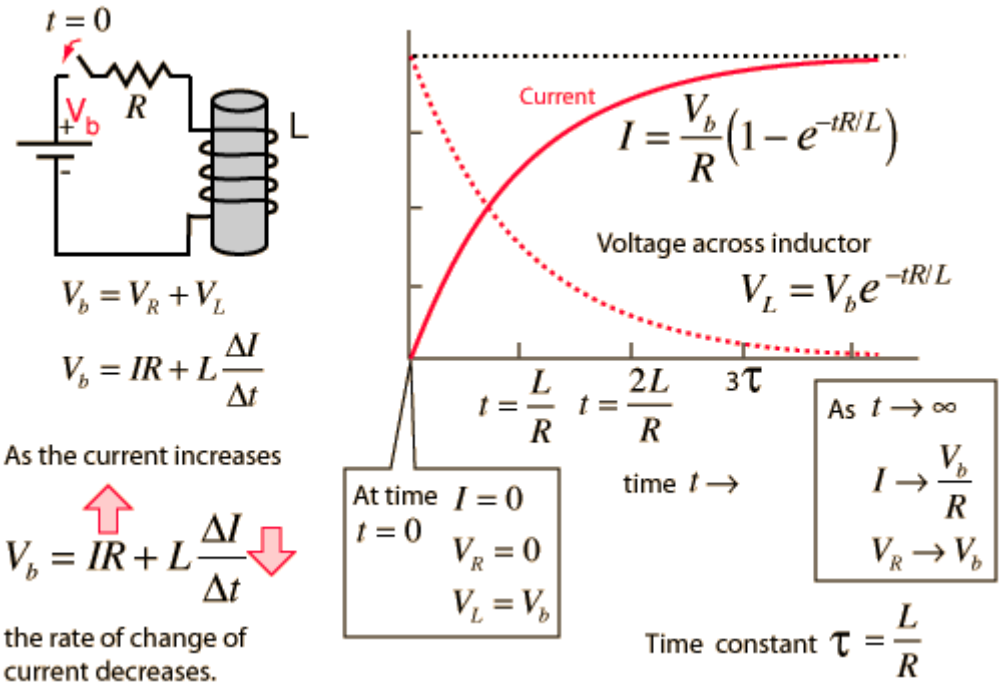


Figure 6 Dynamic behavior of an inductor

For useful notions and examples of the dynamic behavior of the inductor check this web page:

Useful link: http://hyperphysics.phy-astr.gsu.edu/hbase/electric/indtra.html

EXAMPLES

Useful link: https://www.youtube.com/watch?v=lu0Jap0IWQw

CIRCUITS

THEOREMS AND TECHNIQUES FOR THE SOLUTION OF CIRCUITS IN THE TIME DOMAIN

KIRCHHOFF'S CIRCUIT LAWS:

KIRCHHOFF'S CURRENT LAW:

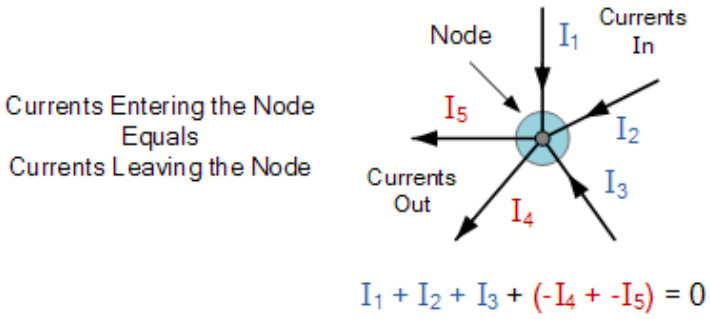


Figure 7 Kirchhoff's current law

Here, the 3 currents entering the node, I_1, I_2, I_3 are all positive in value and the 2 currents leaving the node, I_4 and I_5 are negative in value. Then this means we can also rewrite the equation as;

$$I_1 + I_2 + I_3 - I_4 - I_5 = 0$$

The term Node in an electrical circuit generally refers to a connection or junction of two or more current carrying paths or elements such as cables and components. Also for current to flow either in or out of a node a closed circuit path must exist. We can use Kirchhoff's current law when analysing parallel circuits.

KIRCHHOFF'S VOLTAGE LAW:

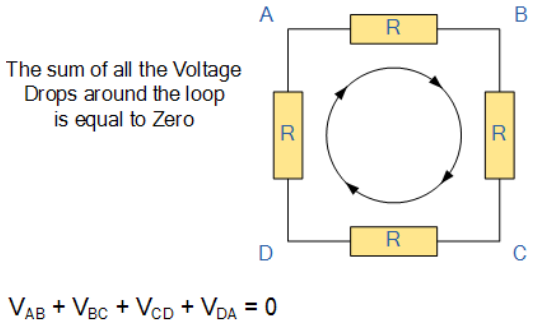


Figure 8 Kirchhoff's voltage law

Starting at any point in the loop continue in the same direction noting the direction of all the voltage drops, either positive or negative, and returning back to the same starting point. It is important to maintain the same direction either clockwise or anti-clockwise or the final voltage sum will not be equal to zero. We can use Kirchhoff's voltage law when analyzing series circuits. When analyzing either DC circuits or AC circuits using Kirchhoffs Circuit Laws a number of definitions and terminologies are used to describe the parts of the circuit being analyzed such as: node, paths, branches, loops and meshes. These terms are used frequently in circuit analysis so it is important to understand them.

For further information:

Useful link: https://en.wikipedia.org/wiki/Kirchhoff's_circuit_laws

MESH-CURRENT AND NODE-VOLTAGE ANALYSIS:

MESH-CURRENT ANALYSIS:

While Kirchhoff´s Laws give us the basic method for analyzing any complex electrical circuit, there are different ways of improving upon this method by using Mesh Current Analysis or Nodal Voltage Analysis that results in a lessening of the math's involved and when large networks are involved this reduction in maths can be a big advantage.

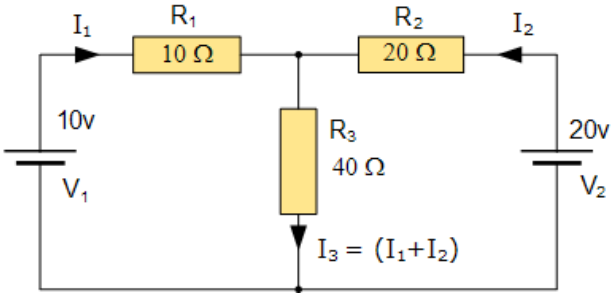


Figure 9 Mesh current analysis

One simple method of reducing the amount of math's involved is to analyze the circuit using Kirchhoff's Current Law equations to determine the currents, I_1 and I_2 flowing in the two resistors.

Then there is no need to calculate the current I_3 as its just the sum of I_1 and I_2. So Kirchhoff's second voltage law simply becomes:

Equation No 1 : $10 = 50I_1 + 40I_2$

Equation No 2 : $20 = 40I_1 + 60I_2$

therefore, one line of math's calculation has been saved.

An easier method of solving the above circuit is by using Mesh Current Analysis or Loop Analysis which is also sometimes called Maxwell´s Circulating Currents method. Instead of labelling the branch currents we need to label each "closed loop" with a circulating current.

As a general rule of thumb, only label inside loops in a clockwise direction with circulating currents as the aim is to cover all the elements of the circuit at least once. Any required branch current may be found from the appropriate loop or mesh currents as before using Kirchhoff´s method.

For example: $i_1 = I_1$, $i_2 = -I_2$ and $I_3 = I_1 - I_2$

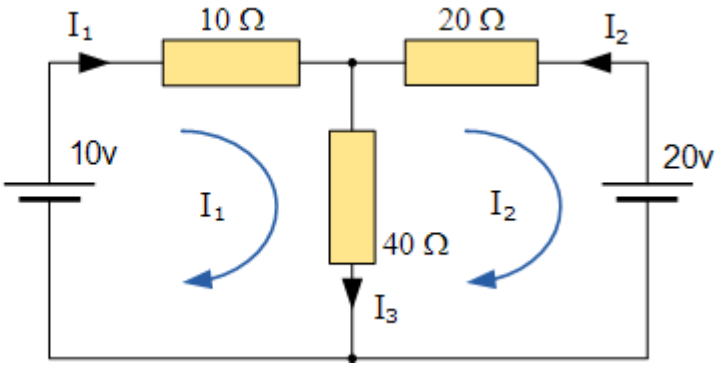
We now write Kirchhoff's voltage law equation in the same way as before to solve them but the advantage of this method is that it ensures that the information obtained from the circuit equations is the minimum required to solve the circuit as the information is more general and can easily be put into a matrix form.

For example, consider the circuit:

$10 = 50I_1 - 40I_2$

$-20 = -40I_1 + 60I_2$

or $[V] = [R] [I]$



These equations can be solved quite quickly by using a single mesh impedance matrix Z. Each element ON the principal diagonal will be "positive" and is the total impedance of each mesh. Where as, each element OFF the principal diagonal will either be "zero" or "negative" and represents the circuit element connecting all the appropriate meshes.

First we need to understand that when dealing with matrices, for the division of two matrices it is the same as multiplying one matrix by the inverse of the other as shown.

$$[V]=[I]\times[R] \quad or \quad [R]\times[I]=[V]$$

$$\begin{bmatrix} 50 & -40 \\ -40 & 60 \end{bmatrix}\times\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}=\begin{bmatrix} 10 \\ -20 \end{bmatrix}$$

$$I=\frac{V}{R} = R^{-1}\times V$$

$$Inverse\ of\ R=\begin{bmatrix} 60 & 40 \\ 40 & 50 \end{bmatrix}$$

$$|R|=(60\times50)-(40\times40)=1400$$

$$\therefore R^{-1}=\frac{1}{1400}\begin{bmatrix} 60 & 40 \\ 40 & 50 \end{bmatrix}$$

having found the inverse of R, as V/R is the same as V x R^{-1}, we can now use it to find the two circulating currents.

$$[I]=\left[R^{-1}\right]\times[V]$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}=\frac{1}{1400}\begin{bmatrix} 60 & 40 \\ 40 & 50 \end{bmatrix}\times\begin{bmatrix} 10 \\ -20 \end{bmatrix}$$

$$I_1=\frac{(60\times10)+(40\times-20)}{1400}=\frac{-200}{1400}=-0.143A$$

$$I_2=\frac{(40\times10)+(50\times-20)}{1400}=\frac{-600}{1400}=-0.429A$$

Where:

[V] gives the total battery voltage for loop 1 and then loop 2

[I] states the names of the loop currents which we are trying to find

[R] is the resistance matrix

[R^{-1}] is the inverse of the [R] matrix

and this gives I_1 as -0.143 Amps and I_2 as -0.429 Amps

As : $I_3 = I_1 - I_2$

The combined current of I_3 is therefore given as: -0.143 – (-0.429) = 0.286 A.

SUMMARY

This "look-see" method of circuit analysis is probably the best of all the circuit analysis methods with the basic procedure for solving Mesh Current Analysis equations is as follows:

1. Label all the internal loops with circulating currents. (I1, I2, …IL etc)

2. Write the [L x 1] column matrix [V] giving the sum of all voltage sources in each loop.

3. Write the [L x L] matrix, [R] for all the resistances in the circuit as follows;

- R_{11} = the total resistance in the first loop.
- R_{nn} = the total resistance in the Nth loop.
- R_{JK} = the resistance which directly joins loop J to Loop K.

4. Write the matrix or vector equation $[V] = [R] \times [I]$ where $[I]$ is the list of currents to be found.

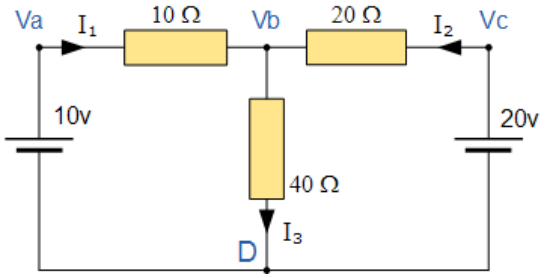
As well as using Mesh Current Analysis, we can also use node analysis to calculate the voltages around the loops, again reducing the amount of mathematics required using just Kirchoff's laws.

For further info check:

Useful link: http://www.electronics-tutorials.ws/dccircuits/dcp_5.html

NODE-VOLTAGE ANALYSIS:

Nodal Voltage Analysis complements the previous mesh analysis in that it is equally powerful and based on the same concepts of matrix analysis. As its name implies, Nodal Voltage Analysis uses the "Nodal" equations of Kirchhoff's first law to find the voltage potentials around the circuit. So by adding together all these nodal voltages the net result will be equal to zero. Then, if there are "n" nodes in the circuit there will be "n-1" independent nodal equations and these alone are sufficient to describe and hence solve the circuit. At each node point write down Kirchhoff's first law equation, that is: "the currents entering a node are exactly equal in value to the currents leaving the node" then express each current in terms of the voltage across the branch. For "n" nodes, one node will be used as the reference node and all the other voltages will be referenced or measured with respect to this common node. For example, consider the circuit from the previous section.



In the above circuit, node D is chosen as the reference node and the other three nodes are assumed to have voltages, Va, Vb and Vc with respect to node D. For example;

$$\frac{(V_a - V_b)}{10} + \frac{(V_c - V_b)}{20} = \frac{V_b}{40}$$

As Va = 10v and Vc = 20v , Vb can be easily found by:

$$\left(1 - \frac{Vb}{10}\right) + \left(1 - \frac{Vb}{20}\right) = \frac{Vb}{40}$$

$$2 = Vb\left(\frac{1}{40} + \frac{1}{20} + \frac{1}{10}\right)$$

$$Vb = \frac{80}{7}V$$

$$\therefore I_3 = \frac{2}{7} \; or \; 0.286 Amps$$

From both Mesh and Nodal Analysis methods we have looked at so far, this is the simplest method of solving this particular circuit. Generally, nodal voltage analysis is more appropriate when there are a larger number of current sources around. The network is then defined as: [I] = [Y] [V] where [I] are the driving current sources, [V] are the nodal voltages to be found and [Y] is the admittance matrix of the network which operates on [V] to give [I].

SUMMARY

The basic procedure for solving Nodal Analysis equations is as follows:

- 1. Write down the current vectors, assuming currents into a node are positive. ie, a (N x 1) matrices for "N" independent nodes.
- 2. Write the admittance matrix [Y] of the network where:
  - Y_{11} = the total admittance of the first node.
  - Y_{22} = the total admittance of the second node.
  - R_{JK} = the total admittance joining node J to node K.
- 3. For a network with "N" independent nodes, [Y] will be an (N x N) matrix and that Ynn will be positive and Yjk will be negative or zero value.
- 4. The voltage vector will be (N x L) and will list the "N" voltages to be found.

For further info check:

Useful link: http://www.electronics-tutorials.ws/dccircuits/dcp_6.html

EXAMPLES:

Useful link: http://www.calvin.edu/~svleest/circuitExamples/NodeVoltageMeshCurrent/

FREQUENCY DOMAIN ANALYSIS:

LAPLACE TRANSFORM PRINCIPLES AND PROPERTIES:

For a review of Laplace transform principles, properties, functions and examples check the relative section in the automatic controls material:

Useful link: http://lpsa.swarthmore.edu/LaplaceXform/FwdLaplace/LaplaceXform.html

LAPLACE APPROACH FOR CIRCUIT ANALYSIS:

Laplace approach for analysis of AC circuit is a very powerful and commonly used method.

To understand the theoretical basis and the power of Laplace approach in circuit analysis check the example proposed on this webpage:

Useful link: http://homepages.cae.wisc.edu/~ece902/LectureNotes/Simulation_1up/lec3c.pdf

For further examples of Laplace domain analysis check this channel:

Useful link: https://www.youtube.com/watch?v=oogQFpvqqLo

GENERALIZATION OF THE THEOREMS FOR THE FREQUENCY DOMAIN:

The methods seen above (mesh-current and node-voltage analysis) can be used also in the frequency domain, with the difference that the quantities must be properly represented in the domain (for example with laplace approach or phasor method) as you found in the material proposed above.

PHASOR METHOD:

In the analysis of AC circuits this method is very powerful and used. For an overview of the mathematical basis and some examples check this link:

Useful link:
https://www.google.it/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=0ahUKEwjsxYnTpbrRAhUPdFAKHY_tC3UQFggaMAA&url=http%3A%2F%2Focw.nctu.edu.tw%2Fcourse%2Fsignals_and_systems_102%2FSAS_20_102.pdf&usg=AFQjCNFJAMgDyulyPkzHjtOlVGKaLmLoxg&sig2=pmUr0OLDLKKL0tKlki1-uw&bvm=bv.143423383,d.ZWM

EXAMPLES:
Useful link: https://www.youtube.com/watch?v=xGeg3QlRLa8

DIODE

INTRODUCTION

For a basic, yet very useful understanding of the diode take a look at this video from Learning Engineering :

Useful link: https://www.youtube.com/watch?v=JNi6WY7WKAI

DESCRIPTION:

The semiconductor diode (*p-n junction*) is an electronic component with two terminals (*bi-pole*). Its function is to allow the current flow in one direction (*called forward direction)* while blocking the flow in the other one *(called reverse direction)*. The electronic symbol clearly recalls its main function: the triangle indicates, as an arrow, the forward direction. The two terminals go under the names of anode(A) and cathode(K)

Next figure compares the electronic symbol of a diode, with its typical real appearance. Notice how the cathode is usually marked with a different colored strip:

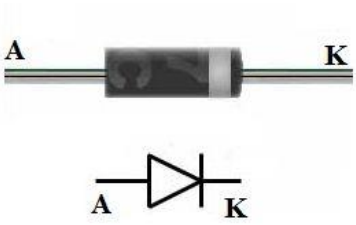


Figure 10 Diode

The mathematical laws governing the behaviour of a diode are quite complex and not easy to manage, hence, in most cases, an ideal model is used. Here is the transcharacteristic of an ideal diode compared to a real one:

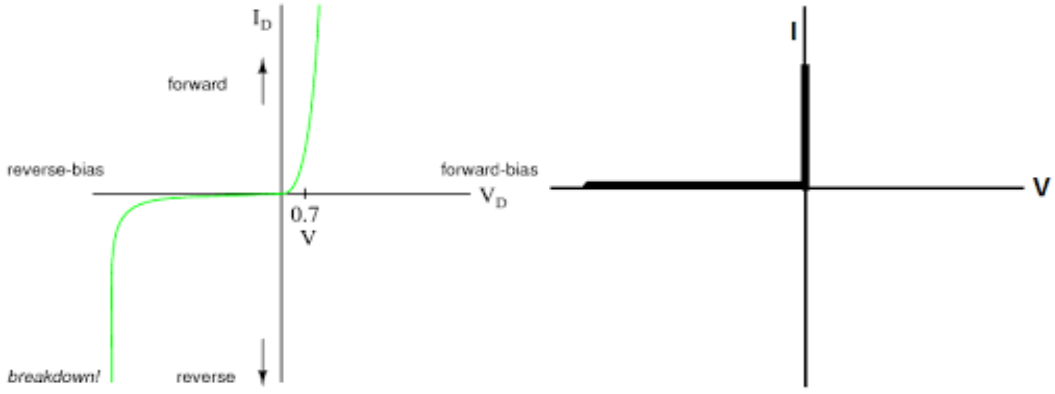


Figure 11 Diode transcharacteristic

In the figure below two circuit are compared: in the first the diode conduces the current and the lamp is on, in the second the diode blocks the current and the lamp is off.

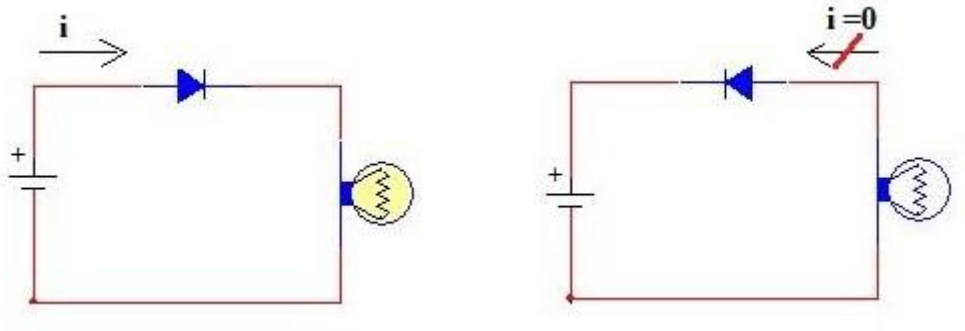
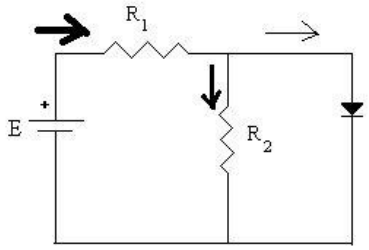


Figure 12 Diode working example

Ideally speaking, the type of diode does not have any influence on the current, which, in direct polarization (diode conducting) is determined by the ratio between the Voltage of the source and the resistance of the battery, while in inverse polarization (diode not conducting) is null. Regarding the voltage, in direct polarization, we will measure a very small voltage drop across the diode (typically 0.5-1V). In inverse polarization, since it is considered as an open circuit, we will measure a voltage across the diode equal to the voltage of the source.

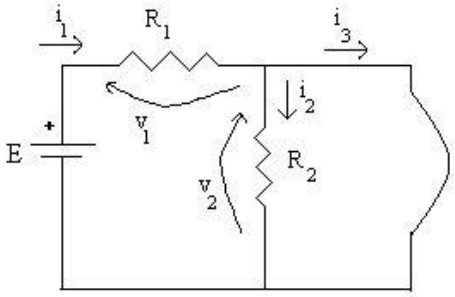
APPLICATIONS

EXAMPLE OF A CIRCUIT WITH IDEAL DIODE:



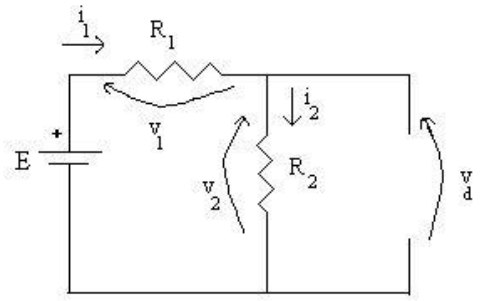
In This configuration the diode is in direct polarization.

Ideally it will behave as a piece of conducting wire and, consequentially, the resistance R2 is short circuited.



I2=0 , V2=0

I1=I3



Now consider this other case:

The diode is in inverse polarization, since the Voltage source forces a current in the reverse direction.

In this configuration it behaves like an open circuit.

I1=I2

Vd=V2

MAIN APPLICATIONS:

Thanks to their unidirectional behaviour with respect to current flow, diodes are used in many applications. One of these is the Voltage rectifier, a circuit that is able to process an alternate input signal (with both positive and negative values) and return as output a signal with only positive or negative values.

SINGLE WAVE RECTIFIER:

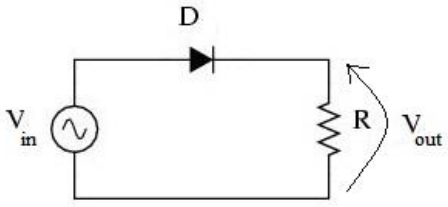


Figure 13Single wave rectifier circuit

For positive values of Vin, the diode is conducting (direct polarization). Considering the ideal model of the diode, it will behave like a short circuit in direct polarization, hence the voltage on the load R is equal to Vin.Viceversa, for negative values of Vin, the diode is in inverse polarization and thus behaves like an open circuit. No current flows in the circuit and the voltage across the load is zero.

The pictures show the waveforms of Vin and Vout in an ideal single wave rectifier:

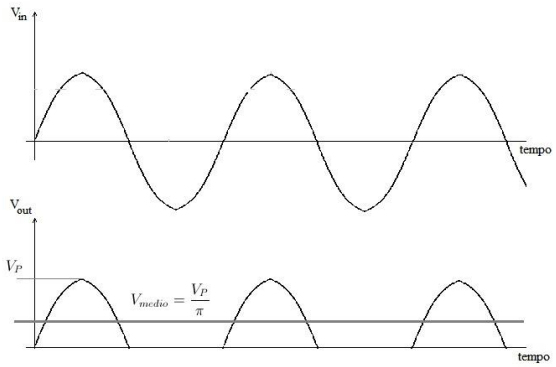


Figure 14 Single wave rectifier waves

Now imagine to connect a capacitor C in parallel to the load R:

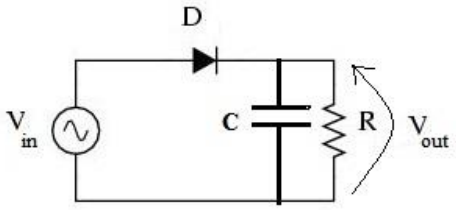


Figure 15 Filtered single wave rectifier

When the voltage of the generator starts decreasing, the capacitor would discharge but it can't discharge through the diode since the current flow in that direction is blocked (the voltage on the capacitor is higher than the voltage of Vin and the diode is in inverse polarization).

The capacitor will then discharge through the load resistance with a time constant tau=RC.

Figure 16 Filtered single wave rectifier waves

As a result, the output voltage is still not countinous but has a very small ripple compared to the wave rectified without the capacitor. The higher is the time constant of the group RC the lesser will be the output ripple.

ZENER

The **zener diode** (or *Zener)* is a particular diode commonly used as voltage stabilizer. Its electronic symbol and typical appearance are shown below (A and K indicate anode and cathode):

APPLICATION

When in **direct polarization**, the zener behaves as a standard diode, it starts to conduct when is applied a voltage higher than a threshold voltage (typically 0.3-0.7V).

In **inverse polarization** the Zener does not conduct, as standard diodes, until a negative threshold voltage is reached, called Zener voltage. This voltage actually corresponds to the breakdown voltage of the standard diodes.

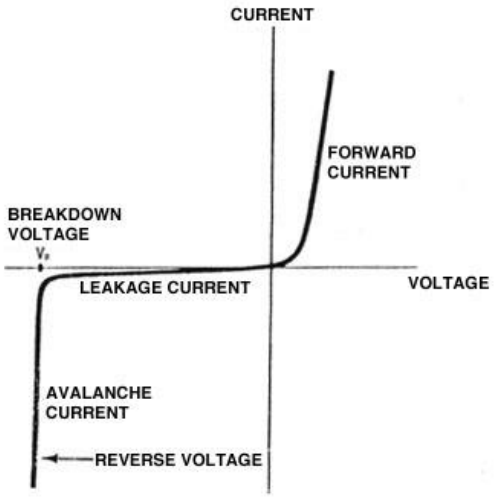


Figure 17 Diode real characteristic

Differently from what happens with standard diodes, the Zener does not get damaged when it reaches the breakdown voltage. In fact it is designed to work in the breakdown region (or Zener region).

EXAMPLE

Let's analyze in detail what happens when the reverse voltage is applied to the diode

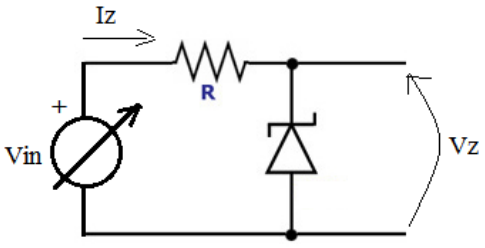


Figure 18 Zener circuit

notes:

Vin represents a voltage source, continuous but variable in time.

The diode is connected in order to be in inverse polarization.

The resistance R is mandatory to protect the diode (it could get burned if undergoing much higher voltage than its zener voltage).

No current flows in the circuit until the source reaches the zener voltage (the diode is an open circuit Iz=0).

When Vin reaches the zener voltage value, the diode starts conducting, allowing a reverse current to flow. The value of this current can be evaluated as follow:

$$I_z = \frac{V_{in} - V_z}{R}$$

Vz is the zener voltage of the diode, it is keeps constant for a given diode, for variable values of Vin. Practically speaking the Zener works as a precise and constant voltage source, that is why it is mostly used as a voltage stabilizer.

If the input voltage is constant we can easily determine the value of the resistance R:

$$R = \frac{V_{in} - V_z}{I_z}$$

The problem is that in the vast majority of cases, the Zener is used, as said before, to stabilize a variable voltage. However the value of R doesn't have to be too high, in order to guarantee a current of at least Izmin.

WITH LOAD…
If we connect a load in parallel to the Zener, the situation gets more complicated:

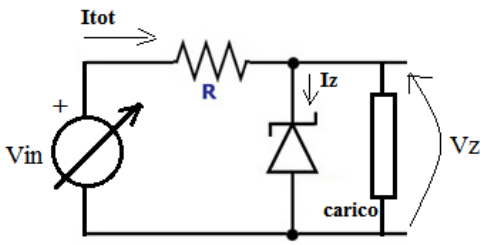


Figure 19 Zener diode with load

In this case we need to know what is the value of the maximum current absorbed by the load. If for example we consider a resistance as a load, this value is easy to evaluate, knowing the value of the resistance:

Iload = Vz/Rload

The total current flowing in the zener will be:

Iz = Itot – Iload

This fact produces a reduction of the current flowing in the diode. This reduction can compromise the working condition of the Zener, since the current could be not sufficient anymore to make it work in the Zener region. For this reason the Zener diodes are suitable to stabilize the voltage on loads with a low current absorption (high resistance loads).

For further information check the website:

Useful link: http://www.elemania.altervista.org/diodi/pn/pn1.html

TRANSISTOR

INTRODUCTION

For a basic, yet very useful understanding of the transistor take a look at this video from Learning Engineering :

Useful link: https://www.youtube.com/watch?v=7ukDKVHnac4&t=133s

DESCRIPTION

The transistor is an electronic component with three terminals. As a first instance we can say that one terminal is used to control the current flowing between the remaining two.

We will name only two famous type of transistor, but the reader must know that there exist a very large number of different transistors, designed for many different applications.

MOSFET TRANSISTOR

The **metal–oxide–semiconductor field-effect transistor** is a type of transistor, mostly used as a linear amplifier or as a *switch*. We will see only examples of applications in which the MOS is used as a switch.

In the following picture is showed its electronic symbol. All three symbols are equivalent: the first is the standard symbol, the second is the simplified symbol, the third is a practical symbol that puts in evidence the presence of a built-in diode, always present:

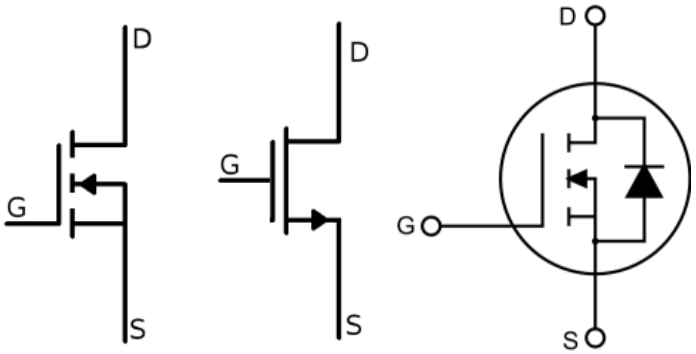


Figure 20 MOSfet circuit symbol

Figure below shows a set of typical characteristic curves for the current ***Ids*** between the drain and source of a MOSFET as a function of the voltage **Vds** for a range of gate voltages, ***Vgs*** (voltage between gate and source).

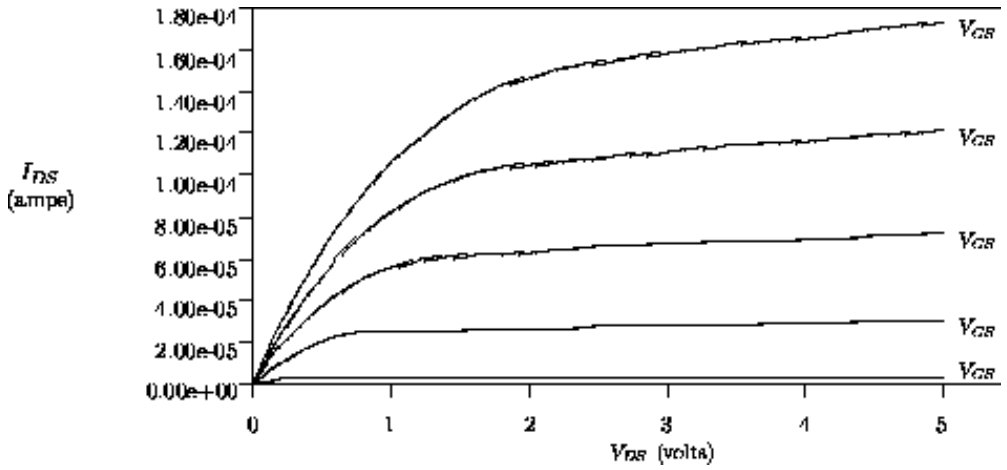


Figure 21 MOS external characteristic

Two regions can be identified in the graph:

In the first region, for low values of Vds, the transistor behaves like an amplifier with a gain that can be considered linear under the assumption of small signals.

In the second region (saturation region), for values of Vds above a certain threshold, the current in the transistor saturates and remains almost constant for every value of Vds.

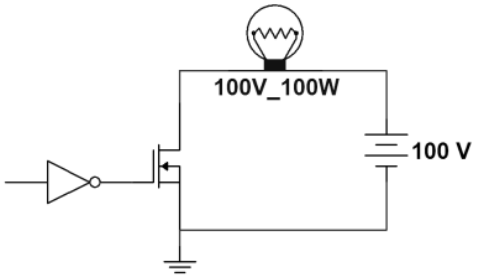
Simplified working principles (as a switch)

The working principle of the MOSfet as a switch is the following:

- If the voltage between Gate and Source Vgs is null, the current entering the Drain Id is null, and the same is for the current coming from Source Is. The transistor behaves like an open switch.
- If the voltage between Gate and Source is higher than a threshold value, a current is able to flow, entering the Drain and coming out from the Source. Typically the voltage drop between D and S is very low (close to 0V). In this second case the transistor behaves like a closed switch (or a very small resistance).

SIMPLE APPLICATION:

Switching on/off a lamp (100W,100V, hence 1A) by means of a logic port (logic ports provides maximum output currents of 10-20 mA but MOSfet transistors absorbs a Gate current that is close to 0A).



If the input is low (0V for logic signals) the current is not able to flow through the MOSfet and the lamp is not supplied, hence switched off.

If the input is high level, the MOS conducts (with a very low resistance value of about 0.5 ohm) and the lamp is switched on.

BJT (BIPOLAR JUNCTION TRANSISTOR)

Differently from MOSfet transistor the BJT is not built with Oxide as an isolation material between the the "control" terminal and the remaining two. It is realized by means of selective doping of three regions in a semiconductor material. According to the doping topology we can have two types of BJT transistor:

The ***npn* BJT** and the ***pnp* BJT**. They are different for the electronic symbol (the different direction of the arrow on the Emitter indicates also the direction of the current flow entering the terminal) and for the direction of currents and voltages as shown in the picture below:

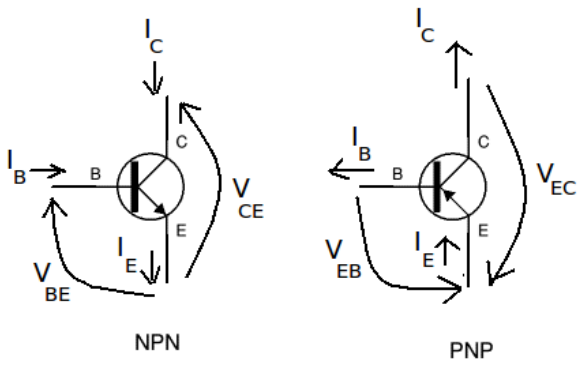
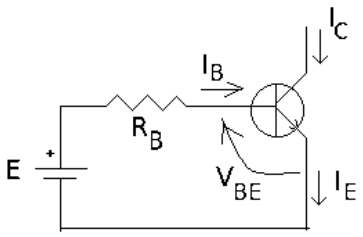


Figure 22 NPN vs PNP transistor

The BJT transistor has three working regions:

- Cut-off region (Vbe<0.6-0.7V) : The BJT does not conduce current, the currents of Base (Ib), Emitter (Ie) and Collector (Ic) are null (or yet very small)
- Active region (Vbe>0.6-0.7V and Vce>0.3-0.4V) : It behaves like a current amplifier, the current in the collector is directly proportional to the current in the base
- Saturation region (Vbe>0.6-0.7V and Vce<0.3-0.4V) : The BJT, ideally, behaves like a piece of wire connecting Emitter and Collector. The proportional relation between Ic and Ib is no more valid.

EXAMPLE



If the voltage of the battery E is higher than the threshold value, (0.6-0.7V) the current Ib can be easily obtained:

$$I_B = \frac{E - V_{BE}}{R_B}$$

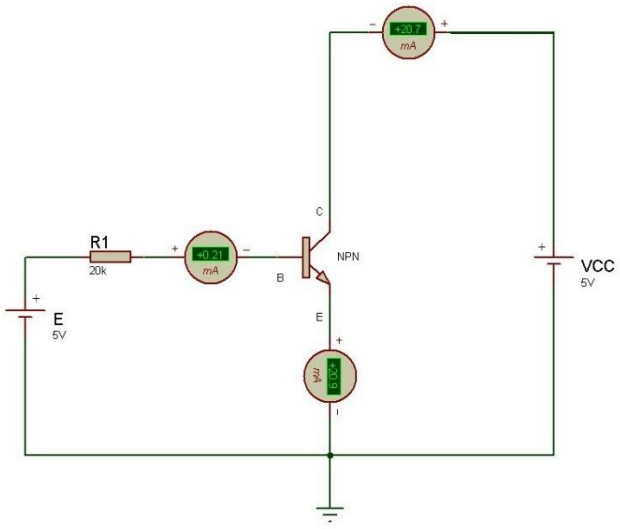
The resistor Rb is mandatory to limit the current entering the Base in order to protect the transistor from being damaged. In this circuit the current Ib is equal to current Ie according to Kirchhoff law, while Ic is null since the collector terminal is floating. The BJT is used as a simple diode.

For example if E = 5 V and RB = 20 kOhm, we will have:

$$I_B = \frac{E - V_{BE}}{R_B} = \frac{5 - 0,7}{20k} = 0,22mA$$

In this case the BJT could be working either in active or saturation region. In other words, the condition between base and emitter is not sufficient to determine the working region of the transistor. For this purpose, we need also to know what happens between Collector and Emitter.

If we apply a positive voltage between Collector and Emitter, things become more interesting:



In this case, the transistor is working in the active region since the following conditions are verified:

- Vbe>0.6-0.7V
- Vce>0.3-0.4V

The current entering the Collector is proportional to the current at the Base:

Ic = ß Ib

The current coming from the emitter can be easily evaluated according to kirchhof's law:

Ie=Ic+Ib

Generally, beta is quite big, that is why the BJT is an excellent current amplifier (remember we are talking about DC current).

WARNING: if Vce goes below 0.3-0.4V the BJT working point moves to the saturation region and the relation between Ic and Ib is no more guaranteed.

For further information check the websites:

Useful link: http://www.vincenzov.net/tutorial/elettronica-di-potenza/MOS.htm

Useful link: http://www.elemania.altervista.org/transistor/bjt/bjt1.html

LOGIC, COMPONENTS AND CIRCUITS

THEOREMS:

Boolean algebra is a different kind of algebra or rather can be said a new kind of algebra which was invented by world famous mathematician George Boole in the year of 1854. He published it in his book "An Investigation of the Laws of Thought". Later using this technique Claude Shannon introduced a new type of algebra which is termed as Switching Algebra. In digital electronics there are several methods of simplifying the design of logic circuits. This algebra is one of these methods. According to George Boole symbols can be used to represent the structure of logical thoughts. This type of algebra deals with the rules or laws, which are known as laws of Boolean algebra by which the logical operations are carried out.

There are also few theorems of Boolean algebra, that are needed to be noticed carefully because these make calculation fastest and easier. Boolean logic deals with only two variables, 1 and 0 by which all the mathematical operations are to be performed.
Boolean algebra or switching algebra is a system of mathematical logic to perform different mathematical operations in binary system. There only three basis binary operations, AND, OR and NOT by which all simple as well as complex binary mathematical operations are to be done. There are many rules in Boolean algebra by which those mathematical operations are done. In Boolean algebra, the variables are represented by English Capital Letter like A, B, C etc and the value of each variable can be either 1 or 0, nothing else. In Boolean algebra an expression given can also be converted into a logic diagram using different logic gates like AND gate, OR gate and NOT gate, NOR gates, NAND gates, XOR gates, XNOR gates etc.

SOME BASIC LOGICAL BOOLEAN OPERATIONS,

AND Operation:

$$0.0 = 0$$
$$0.1 = 0$$
$$1.0 = 0$$
$$1.1 = 1$$

OR Operation:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

Not Operation:

$$\overline{1} = 0$$
$$\overline{0} = 1$$

Some basic laws for Boolean Algebra:

$$\overline{0} = 1, \overline{1} = 0, \; if \; A = 1 \; then \; \overline{A} = 0 \; and \; if \; A = 0, \; then \; \overline{A} = 1.$$

A . 0 = 0 where A can be either 0 or 1.
A . 1 = A where A can be either 0 or 1.
A . A = A where A can be either 0 or 1.
A . $\bar{A}$ = 0 where A can be either 0 or 1.
A + 0 = A where A can be either 0 or 1.
A + 1 = 1 where A can be either 0 or 1.
A + $\bar{A}$ = 1
A + A = A
A + B = B + A where A and B can be either 0 or 1.
A . B = B . A where A and B can be either 0 or 1.
The laws of Boolean algebra are also true for more than two variables like,

CUMULATIVE LAW FOR BOOLEAN ALGEBRA

$$A + B + C = A + C + B = B + A + C = B + C + A = C + A + B = C + B + A$$
$$A.B.C = A.C.B = B.A.C = B.C.A = C.A.B = C.B.A$$

According to Cumulative Law, the order of OR operations and AND operations conducted on the variables makes no differences.

ASSOCIATIVE LAW FOR BOOLEAN ALGEBRA

This law is for several variables, where the OR operation of the variables result is same though the grouping of the variables. This law is quite same in case of AND operators.

$$(A + B) + C = A + (B + C)$$
$$(A.B).C = A.(B.C)$$

DISTRIBUTIVE LAW FOR BOOLEAN ALGEBRA

This law is composed of two operators, AND and OR.

$$A.(B + C) = A.B + A.C$$

Let us show one use of this law to prove the expression.

$$A + B.C = (A + B).(A + C)$$

Proof:

$$\begin{aligned} A + B.C &= A.1 + B.C \ [Since,\ A.1 = A] \\ &= A.(1 + B) + B.C \ [Since,\ B + 1 = 1] \\ &= A.1 + AB + BC \\ &= A.(1 + C) + AB + BC \ [Since,\ A.A = A.1 = A] \\ &= A.(A + C) + B.(A + C) \\ &= (A + B).(A + C) \end{aligned}$$

REDUNDANT LITERAL RULE

$$A + \overline{A}B = A + B$$
$$Similarly,$$
$$A(\overline{A} + B) = AB$$

ABSORPTION LAW FOR BOOLEAN ALGEBRA

$$A + A.B = A(1 + B) = A$$
$$Similarly,\ A(A + B) = A$$

DE MORGAN'S THEOREM

$$\overline{A + B} = \overline{A}\ \overline{B}$$
$$and\ \ \overline{AB} = \overline{A} + \overline{B}$$

For further info on the fundamental theorems of Boolean algebra, governing the logic circuits we are going to talk about, take a look at this page:

Useful link: http://www.electrical4u.com/boolean-algebra-theorems-and-laws-of-boolean-algebra/

LOGIC GATES

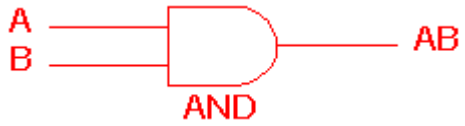
For a basic yet useful understanding of the principal logic gates take a look at this video on youtube from Nurit Kirshenbaum :

Useful link: https://www.youtube.com/watch?v=Xi18hI1LqAA

DESCRIPTION

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

AND GATE



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

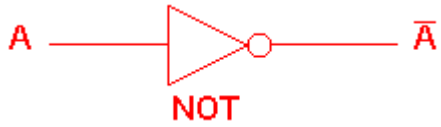
The AND gate is an electronic circuit that gives a high output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB.

OR GATE

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

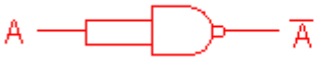
The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

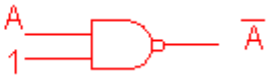
NOT GATE



NOT gate	
A	$\overline{A}$
0	1
1	0

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way.



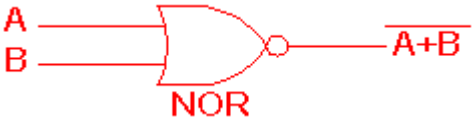


NAND GATE

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

NOR GATE



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

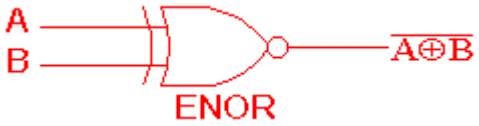
This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

EXOR GATE

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

The 'Exclusive-OR' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation.

EXNOR GATE



2 Input EXNOR gate		
A	B	$\overline{A⊕B}$
0	0	1
0	1	0
1	0	0
1	1	1

The 'Exclusive-NOR' gate circuit does the opposite to the EOR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion.

The NAND and NOR gates are called universal functions since with either one the AND and OR functions and NOT can be generated.

Note:

A function in *sum of products* form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates.

A function in *product of sums* form can be implemented using NOR gates by replacing all AND and OR gates by NOR gates.

LOGIC GATE SYMBOLS

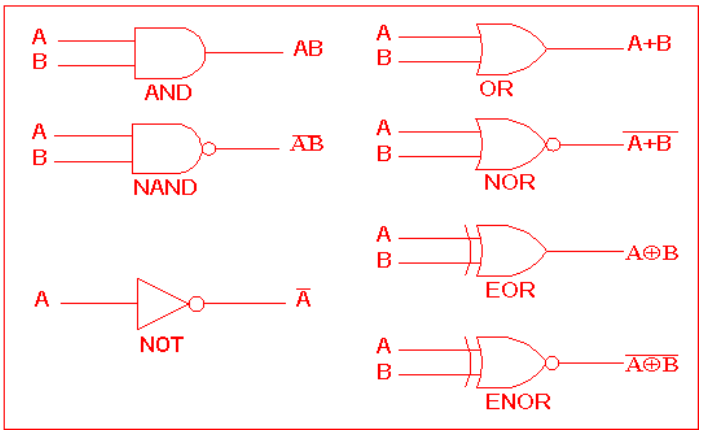


Figure 23 Logic gate symbols

LOGIC GATES REPRESENTATION USING THE TRUTH TABLE

		INPUTS		OUTPUTS					
		A	B	AND	NAND	OR	NOR	EXOR	EXNOR
NOT gate		0	0	0	1	0	1	0	1
A	$\overline{A}$	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0	1	0
1	0	1	1	1	0	1	0	0	1

For further info on the principal logic gates take a look at this page instead:

Useful link: http://www.ee.surrey.ac.uk/Projects/CAL/digital-logic/gatesfunc/

SOME LOGIC CIRCUITS

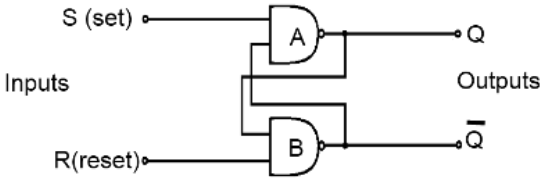
FLIP-FLOP

INTRODUCTION

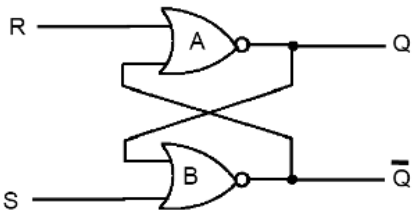
A digital computer needs devices which can store information. A flip flop is a binary storage device. It can store binary bit either 0 or 1. It has two stable states HIGH and LOW i.e. 1 and 0. It has the property to remain in one state indefinitely until it is directed by an input signal to switch over to the other state. It is also called bistable multivibrator. The basic formation of flip flop is to store data. They can be used to keep a record or what value of variable (input, output or intermediate). Flip flop are also used to exercise control over the functionality of a digital circuit i.e. change the operation of a circuit depending on the state of one or more flip flops. These devices are mainly used in situations which require one or more of these three: Operations, storage and sequencing.

LATCH FLIP FLOP

The R-S (Reset Set) flip flop is the simplest flip flop of all and easiest to understand. It is basically a device which has two outputs one output being the inverse or complement of the other, and two inputs. A pulse on one of the inputs to take on a particular logical state. The outputs will then remain in this state until a similar pulse is applied to the other input. The two inputs are called the Set and Reset input (sometimes called the preset and clear inputs). Such flip flop can be made simply by cross coupling two inverting gates either NAND or NOR gate could be used as the first figure shows on RS flip flop using NAND gate and the second figure shows the same circuit using NOR gate.



(a) Latch Flip Flop NAND Gate



(b) RS Latch Flip Flop NOR Gate

Figure 24 Latch Flip Flop

To describe the circuit of the first figure, assume that initially both R and S are at the logic 1 state and that output is at the logic 0 state.

Now, if Q = 0 and R = 1, then these are the states of inputs of gate B, therefore the outputs of gate B is at 1 (making it the inverse of Q i.e. 0). The output of gate B is connected to an input of gate A so

if S = 1, both inputs of gate A are at the logic 1 state. This means that the output of gate A must be 0 (as was originally specified). In other words, the 0 state at Q is continuously disabling gate B so that any change in R has no effect. Also the 1 state at $\overline{Q}$ is continuously enabling gate A so that any change S will be transmitted through to Q. The above conditions constitute one of the stable states of the device referred to as the Reset state since Q = 0. Now suppose that the R-S flip flop in the Reset state, the S input goes to 0. The output of gate A i.e. Q will go to 1 and with Q = 1 and R = 1, the output of gates B ($\overline{Q}$) will go to 0 with $\overline{Q}$ now 0 gate A is disabled keeping Q at 1. Consequently, when S returns to the 1 state it has no effect on the flip flop whereas a change in R will cause a change in the output of gate B. The above conditions constitute the other stable state of the device, called the Set state since Q = 1. Note that the change of the state of S from 1 to 0 has caused the flip flop to change from the Reset state to the Set state.

There is another input condition which has not yet been considered. That is when both the R and S inputs are taken to the logic state 0. When this happens both Q and $\overline{Q}$ will be forced to 1 and will remain so far as long as R and S are kept at 0. However, when both inputs return to 1 there is no way of knowing whether the flip flop will latch in the Reset state or the Set state. The condition is said to be indeterminate because of this indeterminate state great care must be taken when using R-S flip flop to ensure that both inputs are not instructed simultaneously.

Table 1: The truth table for the NAND R-S flip flop

Initial Conditions	**Inputs (Pulsed)**		**Final Output**	
Q	**S**	**R**	**Q**	$\overline{Q}$
1	0	0	indeterminate	
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0
0	0	0	indeterminate	
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1

or more simply shown in Table 2

Table 2: Simple NAND R-S Flip Flop Truth Table

S	R	Q
0	0	indeterminate
0	1	Set (1)
1	0	Reset(0)
1	1	No Change

When NOR gate are used the R and S inputs are transposed compared with the NAND version. Also the stable state when R and S are both 0. A change of state is effected by pulsing the appropriate input to the 1 state. The indeterminate state is now when both R and S are simultaneously at logic 1. Table 3 shows this operation.

Table 3: NOR Gate R-S Flip Flop Truth Table

S	R	Q
0	0	No Change
0	1	Reset (0)
1	0	Set (1)
1	1	Indeterminate

CLOCKED RS FLIP FLOP

The RS latch flip flop required the direct input but no clock. It is very use full to add clock to control precisely the time at which the flip flop changes the state of its output. In the clocked R-S flip flop the appropriate levels applied to their inputs are blocked till the receipt of a pulse from an other source called clock. The flip flop changes state only when clock pulse is applied depending upon the inputs. The basic circuit is shown in Figure 2. This circuit is formed by adding two AND gates at inputs to the R-S flip flop. In addition to control inputs Set (S) and Reset (R), there is a clock input (C) also.

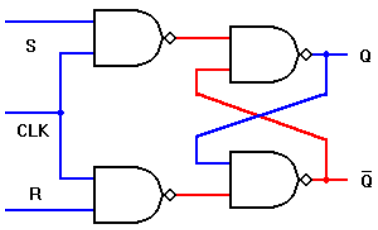


Figure 25 Clocked Flip Flop

Table 4: The truth table for the Clocked R-S flip flop			
Initial Conditions	**Inputs (Pulsed)**		**Final Output**
Q	**S**	**R**	**Q (t + 1)**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

The excitation table for R-S flip flop is very simply derived as given below

Table 5: Excitation table for R-S Flip Flop		
S	**R**	**Q**
0	0	No Change
0	1	Reset (0)
1	0	Set (1)
1	1	Indeterminate

D FLIP FLOP

A D type (Data or delay flip flop) has a single data input in addition to the clock input as shown below:

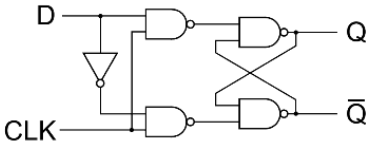


Figure 26 D-Type Flip Flop

Basically, such type of flip flop is a modification of clocked RS flip flop gates from a basic Latch flip flop and NOR gates modify it in to a clock RS flip flop. The D input goes directly to S input and its complement through NOT gate, is applied to the R input. This kind of flip flop prevents the value of D from reaching the output until a clock pulse occurs. The action of circuit is straight forward as follows. When the clock is low, both AND gates are disabled, therefore D can change values without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced equal to D when the clock again goes low, Q retains or stores the last value of D. The truth table for such a flip flop is as given below in table 6.

Table 6: Truth table for D Flip Flop

S	R	Q(t + 1)
0	0	0
0	1	1
1	0	0
1	1	1

The excitation table for D flip flop is very simply derived given as below:

Table 7: Excitation table for D Flip Flop

S	Q
0	0
1	1

JK FLIP FLOP

One of the most useful and versatile flip flop is the JK flip flop the unique features of a JK flip flop are:

- If the J and K input are both at 1 and the clock pulse is applied, then the output will change state, regardless of its previous condition.
- If both J and K inputs are at 0 and the clock pulse is applied there will be no change in the output. There is no indeterminate condition, in the operation of JK flip flop i.e. it has no ambiguous state. The circuit diagram for a JK flip flop is shown below.

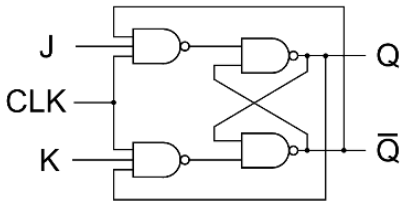


Figura 27 JK-Type Flip Flop

When J = 0 and K = 0

These J and K inputs disable the NAND gates, therefore clock pulse have no effect on the flip flop. In other words, Q returns it last value.

When J = 0 and K = 1

The upper NAND gate is disabled the lower NAND gate is enabled if Q is 1 therefore, flip flop will be reset (Q = 0 , $\overline{Q}$ =1)if not already in that state.

When J = 1 and K = 0

The lower NAND gate is disabled and the upper NAND gate is enabled if $\overline{Q}$ is at 1, As a result we will be able to set the flip flop (Q = 1, $\overline{Q}$ = 0) if not already set

When J = 1 and K = 1

If Q = 0 the lower NAND gate is disabled the upper NAND gate is enabled. This will set the flip flop and hence Q will be 1. On the other hand if Q = 1, the lower NAND gate is enabled and flip flop will be reset and hence Q will be 0. In other words , when J and K are both high, the clock pulses cause the JK flip flop to toggle. Truth table for JK flip flop is shown in table 8.

Table 8: The truth table for the JK flip flop

Initial Conditions	Inputs (Pulsed)		Final Output
Q	**S**	**R**	**Q (t + 1)**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0

Table 8: The truth table for the JK flip flop

Initial Conditions	Inputs (Pulsed)		Final Output
1	1	0	1
1	1	1	0

The excitation table for JK flip flop is very simply derived as given in table 9.

Table 9: Excitation table for JK Flip Flop

S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Toggle

T FLIP FLOP

A method of avoiding the indeterminate state found in the working of RS flip flop is to provide only one input (the T input) such, flip flop acts as a toggle switch. Toggle means to change in the previous stage i.e. switch to opposite state. It can be constructed from clocked RS flip flop be incorporating feedback from output to input as shown in Figure 5.

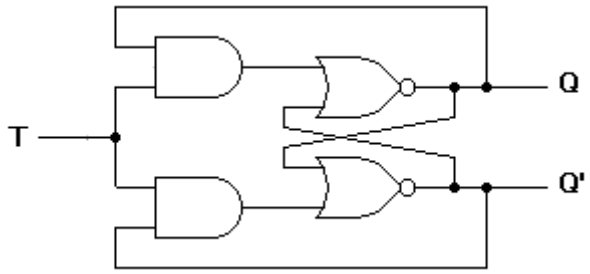


Figure 28 T-Type Flip Flop

Such a flip flop is also called toggle flip flop. In such a flip flop a train of extremely narrow triggers drives the T input each time one of these triggers, the output of the flip flop changes stage. For instance Q equals 0 just before the trigger. Then the upper AND gate is enable and the lower AND gate is disabled. When the trigger arrives, it results in a high S input. This sets the Q output to 1. When the next trigger appears at the point T, the lower AND gate is enabled and the trigger passes through to the R input this forces the flip flop to reset. Since each incoming trigger is alternately changed into the set and reset inputs the flip flop toggles. It takes two triggers to produce one cycle of the output waveform. This means the output has half the frequency of the input stated another

way, a T flip flop divides the input frequency by two. Thus such a circuit is also called a divide by two circuit.

A disadvantage of the toggle flip flop is that the state of the flip flop after a trigger pulse has been applied is only known if the previous state is known. The truth table for a T flip flop is as given table 7.

Table 7: Truth table for T Flip Flop

Q_n	T	$Q_n + 1$
0	0	0
0	1	1
1	0	1
1	1	0

The excitation table for T flip flop is very simply derived as shown in Table 8.

Table 8: Excitation table for T Flip Flop

T	Q
0	Q_n
1	$\overline{Q}_n$

Generally, T flip flop ICs are not available. It can be constructed using JK, RS or D flip flop. Figure 6 shows the relation of T flip flop using JK flip flop.

Figure 6: T Flip Flop Using JK Flip Flop

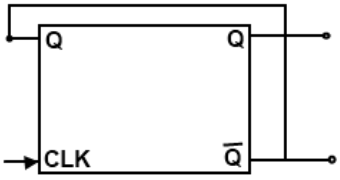


Figure 7: D-type Flip Flop connected as toggle stage

A D-type flip flop may be modified by external connection as a T-type stage as shown in Figure 7. Since the Q logic is used as D-input the opposite of the Q output is transferred into the stage each

clock pulse. Thus the stage having Q - 0 transistors $\overline{Q}$ = 1, Providing a toggle action, if the stage had Q = 1 the clock pulse would result in Q = 0 being transferred, again providing the toggle operation. The D-type flip flop connected as in Figure 6 will thus operate as a T-type stage, complementing each clock pulse.

MASTER SLAVE FLIP FLOP

Figure 8 shows the schematic diagram of master slave J-K flip flop

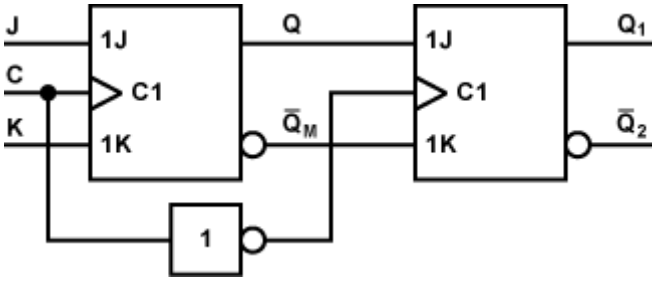


Figure 29 Master-Slave Flip Flop

A master slave flip flop contains two clocked flip flops. The first is called master and the second slave. When the clock is high the master is active. The output of the master is set or reset according to the state of the input. As the slave is incative during this period its output remains in the previous state. When clock becomes low the output of the slave flip flop changes because it become active during low clock period. The final output of master slave flip flop is the output of the slave flip flop. So the output of master slave flip flop is available at the end of a clock pulse.

For further information about the digital flip flop check this page out:

Useful link: http://www.daenotes.com/electronics/digital-electronics/flip-flops-types-applications-woking

For useful video explaining the digital flip flop check these youtube videos:

SR FLIP-FLOP:
Useful link: https://www.youtube.com/watch?v=HZg7fNu-l24&t=13s

D FLIP-FLOP:
Useful link: https://www.youtube.com/watch?v=wcfnEla_Y78

JK FLIP-FLOP:
Useful link: https://www.youtube.com/watch?v=j6krFp511HA

T FLIP-FLOP:
Useful link: https://www.youtube.com/watch?v=wcfnEla_Y78

COUNTERS

INTRODUCTION

For a basic yet useful understanding of Counters take a look at this video on youtube from Neso Academy :

Useful link: https://www.youtube.com/watch?v=iaIu5SYmWVM

ASYNCHRONOUS COUNTERS

Counters, consisting of a number of flip-flops, count a stream of pulses applied to the counter's CK input. The output is a binary value whose value is equal to the number of pulses received at the CK input.

Each output represents one bit of the output word, which, in 74 series counter ICs is usually 4 bits long, and the size of the output word depends on the number of flip-flops that make up the counter. The output lines of a 4-bit counter represent the values 2^0, 2^1, 2^2 and 2^3, or 1,2,4 and 8 respectively. They are normally shown in schematic diagrams in reverse order, with the least significant bit at the left, this is to enable the schematic diagram to show the circuit following the convention that signals flow from left to right, therefore in this case the CK input is at the left.

FOUR BIT ASYNCHRONOUS UP COUNTER

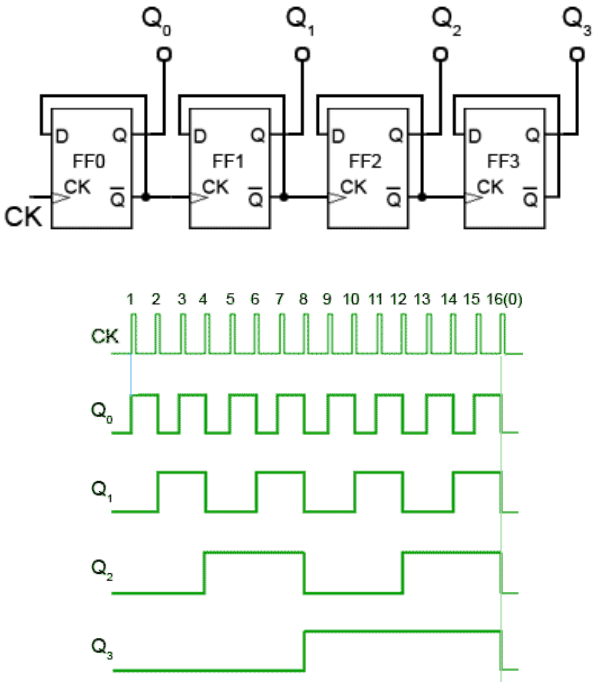


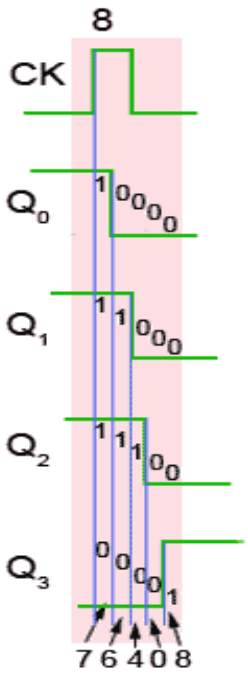
Figure 30 4-bits counter and related waveforms

The upper figure shows a 4 bit asynchronous up counter built from four positive edge triggered D type flip-flops connected in toggle mode. Clock pulses are fed into the CK input of FF0 whose output, Q_0 provides the 2^0 output for FF1 after one CK pulse. The rising edge of the Q output of each flip-flop triggers the CK input of the next flip-flop at half the frequency of the CK pulses applied to its input.

The Q outputs then represent a four-bit binary count with Q_0 to Q_3 representing 2^0 (1) to 2^3 (8) respectively. Assuming that the four Q outputs are initially at 0000, the rising edge of the first CK pulse applied will cause the output Q_0 to go to logic 1, and the next CK pulse will make Q_0 output return to logic 0, and at the same time Q_0 will go from 0 to 1. As Q_0 (and the CK input of FF1 goes high) this will now make Q_1 high, indicating a value of 2^1 (2_{10}) on the Q outputs. The next (third) CK pulse will cause Q_0 to go to logic 1 again, so both Q_0 and Q_1 will now be high, making the 4-bit output 1100_2 (3_{10} remembering that Q_0 is the least significant bit). The fourth CK pulse will make both Q_0 and Q_1 return to 0 and as Q_1 will go high at this time, this will toggle FF2, making Q_2 high and indicating 0010_2 (4_{10}) at the outputs. Reading the output word from right to left, the Q outputs therefore continue to represent a binary number equalling the number of input pulses received at the CK input of FF0. As this is a four-stage counter the flip-flops will continue to toggle in sequence and the four Q outputs will output a sequence of binary values from 0000_2 to 1111_2 (0 to 15_{10}) before the output returns to 0000_2 and begins to count up again as illustrated by the waveforms.

FOUR BIT ASYNCHRONOUS DOWN COUNTER

To convert the up counter to count DOWN instead, is simply a matter of modifying the connections between the flip-flops. By taking both the output lines and the CK pulse for the next flip-flop in sequence from the Q output as shown in the upper figure a positive edge triggered counter will count down from 1111_2 to 0000_2. Although both up and down counters can be built, using the asynchronous method for propagating the clock, they are not widely used as counters as they become unreliable at high clock speeds, or when a large number of flip-flops are connected together to give larger counts, due to the clock ripple effect.



CLOCK RIPPLE

The figure shows how the propagation delays created by the gates in each flip-flop (indicated by the blue vertical lines) add, over a number of flip-flops, to form a significant amount of delay between the time at which the output changes at the first flip flop (the least significant bit), and the last flip flop (the most significant bit). As the Q_0 to Q_3 outputs each change at different times, a number of different output states occur as any particular clock pulse causes a new value to appear at the outputs. At CK pulse 8 for example, the outputs Q_0 to Q_3 should change from 1110_2 (7_{10}) to 0001_2 (8_{10}), however what really happens that the outputs change, over a period of around 400 to 700ns, in the following sequence:

- $1110_2 = 7_{10}$
- $0110_2 = 6_{10}$
- $0010_2 = 4_{10}$
- $0000_2 = 0_{10}$
- $0001_2 = 8_{10}$

At CK pulses other that pulse 8 of course, different sequences will occur, therefore there will be periods, as a change of value ripples through the chain of flip-flops, when unexpected values appear at the Q outputs for a very short time. However this can cause problems when a particular binary value is to be selected, as in the case of a decade counter, which must count from 0000_2 to 1001_2 (9_{10}) and then reset to 0000_2 on a count of 1010_2 (10_{10}). These short-lived logic values will also cause a series of very short spikes on the Q outputs, as the propagation delay of a single flip-flop is only about 100 to 150ns. These spikes are called ‘runt spikes’ and although they may not all reach to full logic 1 value every time, as well as possibly causing false counter triggering, they must also be considered as a possible cause of interference to other parts of the circuit. Although this problem prevents the circuit being used as a reliable counter, it is still valuable as a simple and effective frequency divider, where a high frequency oscillator provides the input and each flip-flop in the chain divides the frequency by two.

SYNCHRONOUS COUNTERS

The synchronous counter provides a more reliable circuit for counting purposes, and for high-speed operation, as the clock pulses in this circuit are fed to every flip-flop in the chain at exactly the same time. Synchronous counters use JK flip-flops, as the programmable J and K inputs allow the toggling of individual flip-flops to be enabled or disabled at various stages of the count. Synchronous counters therefore eliminate the clock ripple problem, as the operation of the circuit is synchronized to the CK pulses, rather than flip-flop outputs.

SYNCHRONOUS UP COUNTER

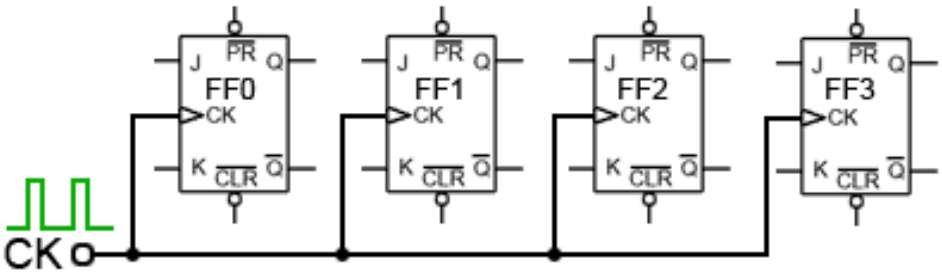
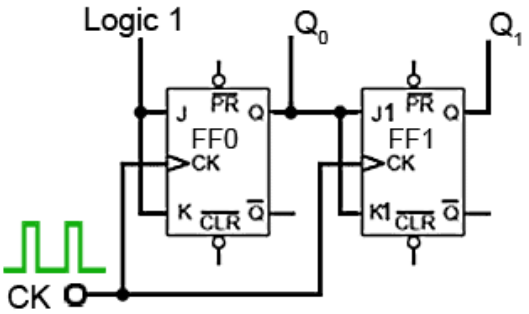


Figure 31 Synchronous up-counter

The figure shows how the clock pulses are applied in a synchronous counter. Notice that the CK input is applied to all the flip-flops in parallel. Therefore, as all the flip-flops receive a clock pulse at the same instant, some method must be used to prevent all the flip-flops changing state at the same time. This of course would result in the counter outputs simply toggling from all ones to all zeros, and back again with each clock pulse. However, with JK flip-flops, when both J and K inputs are logic 1 the output toggles on each CK pulse, but when J and K are both at logic 0 no change takes place.



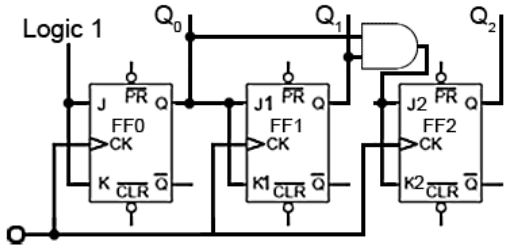
The figure shows two stages of a synchronous counter. The binary output is taken from the Q outputs of the flip-flops. Note that on FF0 the J and K inputs are permanently wired to logic 1, so Q_0 will change state (toggle) on each clock pulse. This provides the 'ones' count for the least significant bit. On FF1 the J1 and K1 inputs are both connected to Q_0 so that FF1 output will only be in toggle mode when Q_0 is also at logic 1. As this only happens on alternate clock pulses, Q_1 will only toggle on even numbered clock pulses giving a 'twos' count on the Q_1 output.

Table 5.6.1

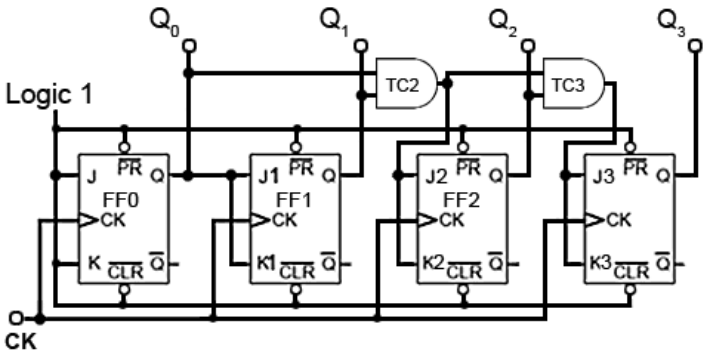
CK	Q_0	Q_1	J1	K1	After the CK pulse
0	0	0	0	0	No CK pulses yet
1	1	0	1	1	Q_0 toggles making J1 & K1 = 1
2	0	1	0	0	Q_0 & Q_1 toggle making J1 & K1 = 0
3	1	1	1	1	Only Q_0 toggles making J1 & K1 = 1
4	0	0	0	0	Q_0 & Q_1 toggle making J1 & K1 = 0

The table shows this action, where it can be seen that Q_1 toggles on the clock pulse only when J1 and K1 are high, giving a two bits binary count on the Q outputs, (where Q_0 is the least significant bit).

In adding a third flip flop to the counter however, direct connection from J and K to the previous Q_1 output would not give the correct count. Because Q_1 is high at a count of 2_{10} this would mean that FF2 would toggle on clock pulse three, as J2 and K2 would be high. Therefore ,clock pulse 3 would give a binary count of 111_2 or 7_{10} instead of 4_{10}.



To prevent this problem an AND gate is used, as shown in the above figure to ensure that J2 and K2 are high only when both Q_0 and Q_1 are at logic 1 (i.e. at a count of three). Only when the outputs are in this state will the next clock pulse toggle Q_2 to logic 1. The outputs Q_0 and Q_1 will of course return to logic 0 on this pulse, so giving a count of 001_2 or 4_{10} (with Q_0 being the least significant bit).



The figure shows the additional gating for a four-stages synchronous counter. Here FF3 is put into toggle mode by making J3 and K3 logic 1, only when Q_0 Q_1 and Q_2 are all at logic 1. Q_3 therefore will not toggle to its high state until the eighth clock pulse, and will remain high until the sixteenth clock pulse. After this pulse, all the Q outputs will return to zero. Note that for this basic form of the synchronous counter to work, the PR and CLR inputs must also be all at logic 1, (their inactive state) as shown in the above figure

Table 5.6.2								
CK	Q_3	Q_2	Q_1	Q_0	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
3	0	0	1	1	1	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	1
11	1	0	1	1	0	1	0	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0
14	1	1	1	0	0	0	0	1
15	1	1	1	1	0	0	0	0

SYNCHRONOUS DOWN COUNTER

Converting the synchronous up counter to count down is simply a matter of reversing the count. If all of the ones and zeros in the 0 to 15_{10} sequence shown in Table 5.6.2 are complemented, (shown with a pink background) the sequence becomes 15_{10} to 0.

DOWN COUNTER CIRCUIT

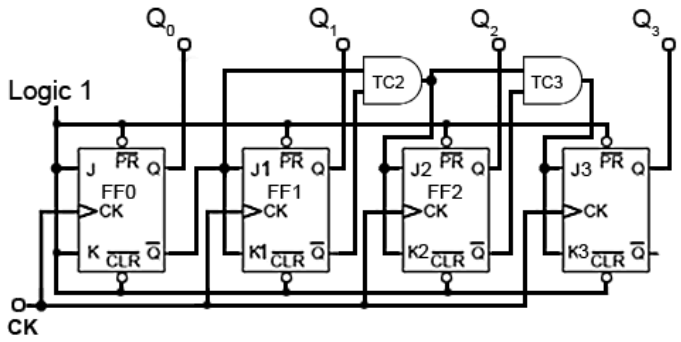


Figure 32 Synchronous down counter

As every Q output on the J flip-flops has its complement on Q, all that is needed to convert the up counter in Fig. 5.6.8 to the down counter shown in the above figure is to take the JK inputs for FF1

from the Q output of FF0 instead of the Q output. Gate TC2 now takes its inputs from the Q outputs of FF0 and FF1, and TC3 also takes its input from FF2 Q output.

UP/DOWN COUNTER

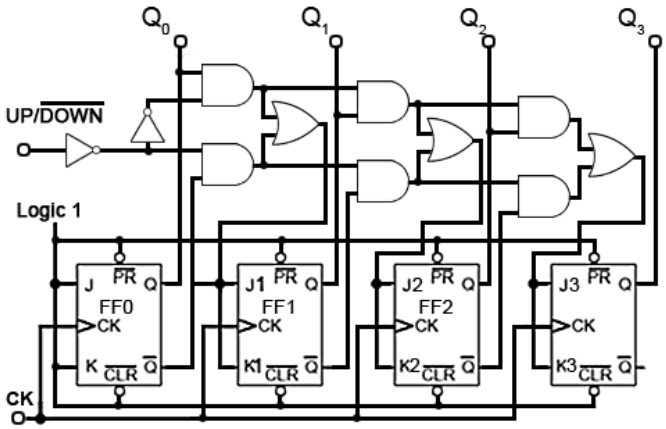


Figure 33 U/D counter

The figure illustrates how a single input, called (UP/DOWN) can be used to make a single counter count either up or down, depending on the logic state at the UP/DOWN input. The Q and Q outputs of flip-flops FF0, FF1 and FF2 are connected to what are, in effect, the A and B data inputs of the data selectors. If the control input is at logic 1 then the CK pulse to the next flip-flop is fed from the Q output, making the counter an UP counter, but if the control input is 0 then CK pulses are fed from Q and the counter is a DOWN counter.

SYNCHRONOUS BCD UP COUNTER

A typical use of the CLR inputs is illustrated in the BCD Up Counter. The counter outputs Q_1 and Q_3 are connected to the inputs of a NAND gate, the output of which is taken to the CLR inputs of all four flip-flops. WhenQ_1 and Q_3 are both at logic 1, the output terminal of the limit detection NAND gate (LD1) will become logic 0 and reset all the flip-flop outputs to logic 0. Because the first time Q_1 and Q_3 are both at logic 1 during a 0 to 1510 count is at a count of ten (10102), this will cause the counter to count from 0 to 910 and then reset to 0, omitting 10_{10} to 15_{10}. The circuit is therefore a BCD_{8421} counter, an extremely useful device for driving numeric displays via a BCD to 7-segment decoder etc. However by re-designing the gating system to produce logic 0 at the CLR inputs for a different maximum value, any count other than 0 to 15 can be achieved.

COUNTER IC INPUTS AND OUTPUTS

Although synchronous counters can be, and are built from individual JK flip-flops, in many circuits they will be ether built into dedicated counter ICs, or into other large scale integrated circuits (LSICs). For many applications the counters contained within ICs have extra inputs and outputs added to increase the counters versatility. The differences between many commercial counter ICs are basically the different input and output facilities offered. Some of which are described below. Notice that many of these inputs are active low; this derives from the fact that in earlier TTL devices any unconnected input would float up to logic 1 and hence become inactive. However leaving inputs un-connected is not good practice, especially CMOS inputs, which float between logic states, and could easily be activated to either valid logic state by random noise in the circuit, therefore ANY unused input should be permanently connected to its inactive logic state.

ENABLE INPUTS

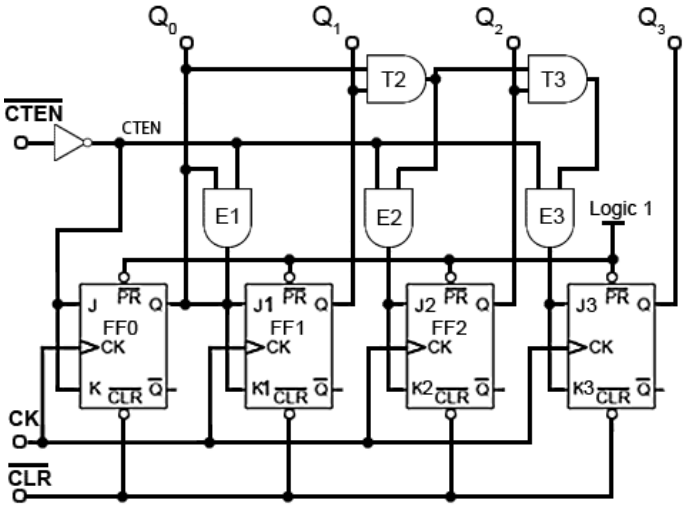


Figure 33 Enable inputs

ENABLE (EN) inputs on counter ICs may have a number of different names, e.g. Chip Enable (CE), Count Enable (CTEN), Output Enable (ON) etc., each denoting the same or similar functions. Count Enable (CTEN) for example, is a feature on counter integrated circuits, and in the synchronous counter illustrated in the above figure, is an active low input. When it is set to logic 1, it will prevent the count from progressing, even in the presence of clock pulses, but the count will continue normally when CTEN is at logic 0. A common way of disabling the counter, whilst retaining any current data on the Q outputs, is to inhibit the toggle action of the JK flip-flops whilst CTEN is inactive (logic 1), by making the JK inputs of all the flip-flops logic 0. However, as the logic states of the JK inputs of FF1, FF2 and FF3 depend on the state of the previous Q output, either directly or via gates T2 and T3, in order to preserve the output data, the Q outputs must be isolated from the JK inputs whenever CTEN is logic 1, but the Q outputs must connect to the JK inputs when CTEN is at logic 0 (the count enabled state). This is achieved by using the extra (AND) enable gates, E1, E2 and E3, each of which have one of their inputs connected to CTEN (the inverse of CTEN). When the count is disabled, CTEN and therefore one of the inputs on each of , E1, E2 and E3 will be at logic 0, which will cause these enable gate outputs, and the flip-flop JK inputs to also be at logic 0, whatever logic states are present on the Q outputs, and also at the other enable gate inputs. Therefore whenever CTEN is at logic 1 the count is disabled. When CTEN is at logic 0 however, CTEN will be logic 1 and E1, E2 and E3 will be enabled, causing whatever logic state is present on the Q outputs to be passed to the JK inputs. In this condition, when the next clock pulse is received at the CK input the flip-flops will toggle, following their normal sequence.

ASYNCHRONOUS PARALLEL LOAD

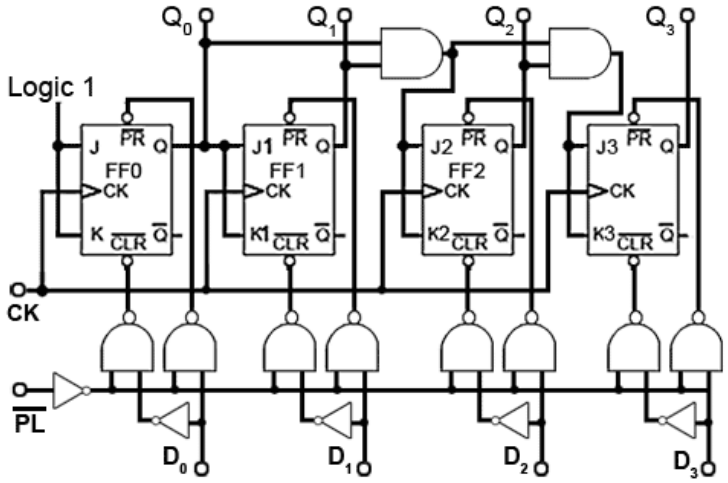


Figure 34 Asynchronous parallel load

While common PR and CLR inputs can produce outputs of 0000 or 1111, a PARALLEL LOAD (PL) input will allow any value to be loaded into the counter. Using a separate DATA input for each flip-flop, and a small amount of extra logic, a logic 0 on the PL will load the counter with any pre-determined binary value before the start of, or during the count. A method of achieving asynchronous parallel loading on a synchronous counter is shown in the above figure.

LOAD OPERATION

The binary value to be loaded into the counter is applied to inputs D_0 to D_3 and a logic 0 pulse is applied to the PL input. This logic 0 is inverted and applied to one input of each of the eight NAND gates to enable them. If the value to be loaded into a particular flip-flop is logic 1, this makes the inputs of the right hand NAND gate 1,1 and due to the inverter between the pair of NAND gates for that particular input, the left hand NAND gate inputs will be 1,0. The result of this is that logic 0 is applied to the flip-flop PR input and logic 1 is applied to the CLR input. This combination sets the Q output to logic 1, the same value that was applied to the D input. Similarly, if a D input is at logic 0 the output of the left hand NAND gate of the pair will be Logic 0 and the right hand gate output will be logic 1, which will clear the Q output of the flip-flop. Because the PL input is common to each pair of load NAND gates, all four flip-flops are loaded simultaneously with the value, either 1 or 0 present at its particular D input.

MULTIPLE INPUTS AND OUTPUTS

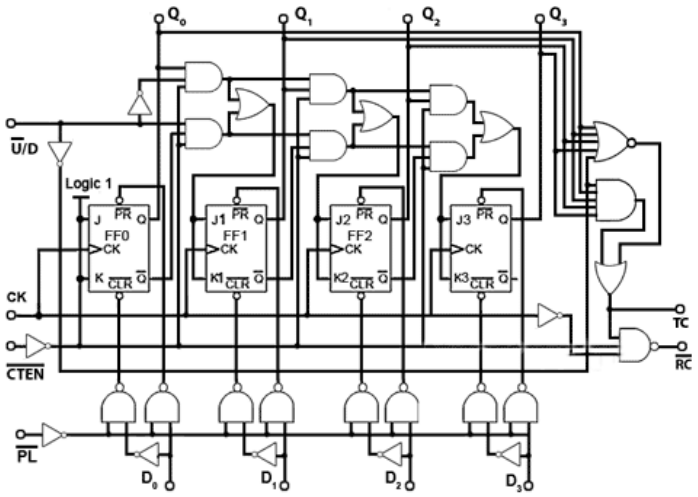


Figure 35 Multiple inputs and outputs

Modifications such as those described in this module make the basic synchronous counter much more versatile. Both TTL and CMOS synchronous counters are available in the 74 series of ICs containing usually 4-bit counters with these and other modifications for a wide variety of applications. The above figure shows how all the input functions described above, plus some important outputs such as Ripple Carry (RC) and Terminal Count (TC) can be combined to form a single synchronous counter IC. A typical single synchronous IC such as the 74HC191 four-bit binary up/down counter also uses these input and output functions, which are designated on NXP versions as follows:

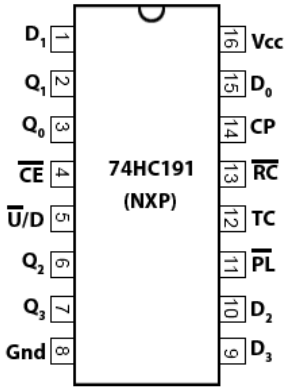
Inputs

• D_0, D_1, D_2 and D_3 (Load inputs) - A 4 bit binary number may be loaded into the counter via these inputs when the Parallel Load input PL is at logic 0.

• CE (Count Enable) - Allows the count to proceed when at 0. Stops count without resetting when at logic 1

• U/D (Up/Down) - Counts up when 0, down when at logic 1.

• CP - Clock Pulse input.



Outputs

• Q_0, Q_1, Q_2 and Q_3 - Four bit binary output.

• TC (Terminal Count) - Also called MAX/MIN in some versions, gives a logic 1 pulse, equal in width to one full clock cycle, at each change over of the most significant bit (signifying that the count has overflowed beyond the end of an up or down count). TC can be used to detect the end of an up or down count, and as well as being available as an output, TC is used internally to generate the Ripple Carry output.

• RC (Ripple Carry) - Outputs a logic 0 pulse, equal in width to the low portion of the clock cycle at the end of a count, and when connected to the clock input of another 74HC191 IC it acts as a 'carry' to the next counter.

CASCADING SYNCHRONOUS COUNTERS

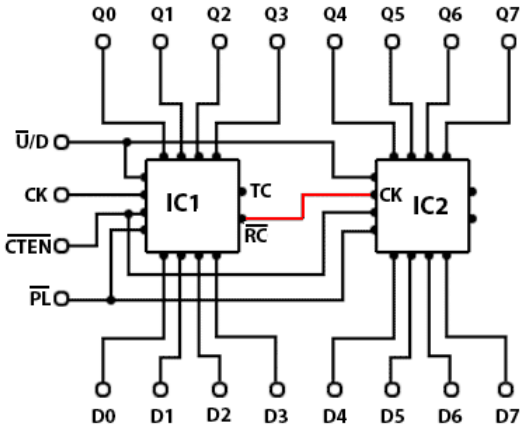


Figure 36 Cascading synchronous counters

Connecting Synchronous counters in cascade, to obtain greater count ranges, is made simple in ICs such as the 74HC191 by using the ripple carry (RC) output of the IC counting the least significant 4 bits, to drive the clock input of the next most significant IC, as show in red in figure. Although it may appear that either the TC or the RC outputs could drive the next clock input, the TC output is not intended for this purpose, as timing issues can occur.

SYNCHRONOUS VS. ASYNCHRONOUS COUNTERS

Although synchronous counters have a great advantage over asynchronous or ripple counters in regard to reducing timing problems, there are situations where ripple counters have an advantage over synchronous counters. When used at high speeds, only the first flip-flop in the ripple counter chain runs at the clock frequency. Each subsequent flip-flop runs at half the frequency of the previous one. In synchronous counters, with every stage operating at very high clock frequencies, stray capacitive coupling between the counter and other components and within the counter itself is more likely occur, so that in synchronous counters interference can be transferred between different stages of the counter, upsetting the count if adequate decoupling is not provided. This problem is reduced in ripple counters due to the lower frequencies in most of the stages. Also, because the clock pulses applied to synchronous counters must charge, and discharge the input capacitance of every flip-flop simultaneously; synchronous counters having many flip-flops will cause large pulses of charge and discharge current in the clock driver circuits every time the clock changes logic state. This can also cause unwelcome spikes on the supply lines that could cause problems elsewhere in the digital circuitry. This is less of a problem with asynchronous counters, as the clock is only driving the first flip-flop in the counter chain. Asynchronous counters are mostly used for frequency division applications and for generating time delays. In either of these applications the timing of individual outputs is not likely to cause a problem to external circuitry, and the fact that most of the stages in the counter run at much lower frequencies than the input clock, greatly reduces any problem of high frequency noise interference to surrounding components.

For more check this page:

Useful link: http://www.learnabout-electronics.org/Digital/dig56.php

MULTIPLEXER

INTRODUCTION

For a basic yet useful understanding of the principal logic gates take a look at this video on youtube from Neso Academy :

Useful link: https://www.youtube.com/watch?v=FKvnmxte98A

In the channel the reader can find also example of multiplexer implementations by means of logic components.

DESCRIPTION

The *multiplexer*, shortened to “MUX” or “MPX”, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called “channels” one at a time to the output. Multiplexers, or MUX’s, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET’s or relays to switch one of the voltage or current inputs through to a single output.

The most basic type of multiplexer device is that of a one-way rotary switch as shown.

BASIC MULTIPLEXING SWITCH

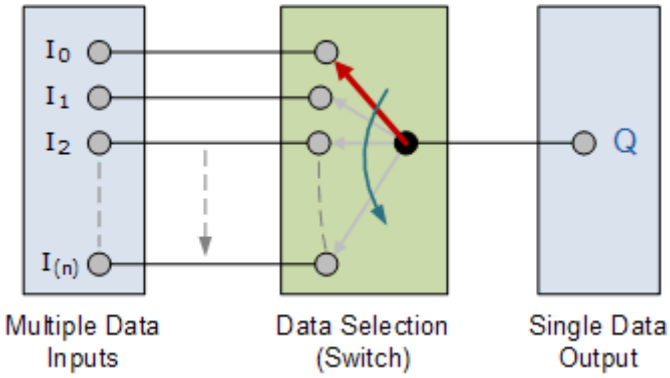


Figure 37 Basic multiplexing switch

The rotary switch, also called a wafer switch as each layer of the switch is known as a wafer, is a mechanical device whose input is selected by rotating a shaft. In other words, the rotary switch is a manual switch that you can use to select individual data or signal lines simply by turning its inputs "ON" or "OFF". So how can we select each data input automatically using a digital device.

In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays. They are used as one method of reducing the number of logic gates required in a circuit design or when a single data line or data bus is required to carry two or more different digital signals. For example, a single 8-channel multiplexer. Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called *control lines* and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2^n data input lines and a number of "control" inputs that correspond with the number of data inputs. Note that multiplexers are different in operation to *Encoders*. Encoders are able to switch an n-bit input pattern to multiple output lines that represent the binary coded (BCD) output equivalent of the active input. We can build a simple 2-line to 1-line (2-to-1) multiplexer from basic logic NAND gates as shown.

2-INPUT MULTIPLEXER DESIGN

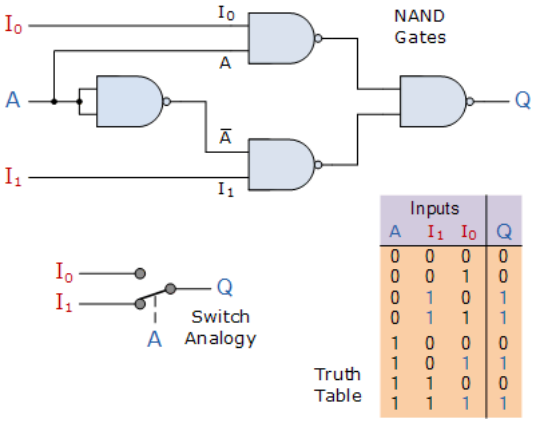


Figure 38 2-input multiplexer design

The input A of this simple 2-1 line multiplexer circuit constructed from standard NAND gates acts to control which input (I_0 or I_1) gets passed to the output at Q. From the truth table above, we can see that when the data select input, A is LOW at logic 0, input I_1 passes its data through the NAND gate multiplexer circuit to the output, while input I_0 is blocked. When the data select A is HIGH at logic 1, the reverse happens and now input I_0 passes data to the output Q while input I_1 is blocked. So by the application of either a logic "0" or a logic "1" at A we can select the appropriate input, I_0 or I_1 with the circuit acting a bit like a single pole double throw (SPDT) switch. As we only have one control line, (A) then we can only switch 2^1 inputs and in this simple example, the 2-input multiplexer connects one of two 1-bit sources to a common output, producing a 2-to-1-line multiplexer. We can confirm this in the following Boolean expression:

$$Q = A.I_0.I_1 + A.I_0.I_1 + A.I_0.I_1 + A.I_0.I_1$$

And for our 2-input multiplexer circuit above, this can be simplified too:

$$Q = A.I_1 + A.I_0$$

We can increase the number of data inputs to be selected further simply by following the same procedure and larger multiplexer circuits can be implemented using smaller 2-to-1 multiplexers as their basic building blocks. So for a 4-input multiplexer we would therefore require two data select lines as 4-inputs represents 2^2 data control lines give a circuit with four inputs, I_0, I_1, I_2, I_3 and two data select lines A and B as shown.

4-TO-1 CHANNEL MULTIPLEXER

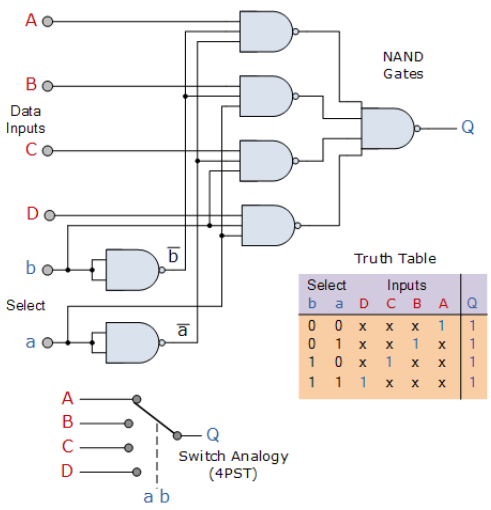


Figure 39 4-input multiplexer schematic

The Boolean expression for this 4-to-1 Multiplexer above with inputs A to D and data select lines a, b is given as:

$$Q = abA + abB + abC + abD$$

In this example at any one instant in time only ONE of the four analogue switches is closed, connecting only one of the input lines A to D to the single output at Q. As to which switch is closed depends upon the addressing input code on lines "a" and "b", so for this example to select input B to the output at Q, the binary input address would need to be "a" = logic "1" and "b" = logic "0".

Then we can show the selection of the data through the multiplexer as a function of the data select bits as shown.

MULTIPLEXER INPUT LINE SELECTION

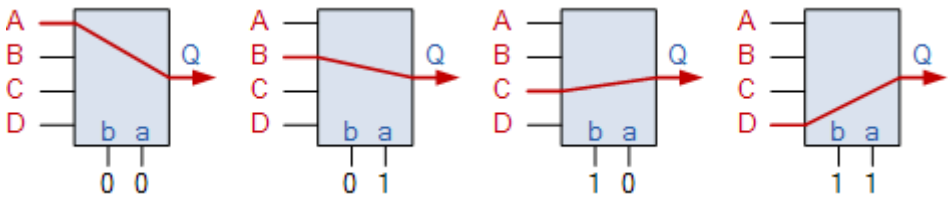
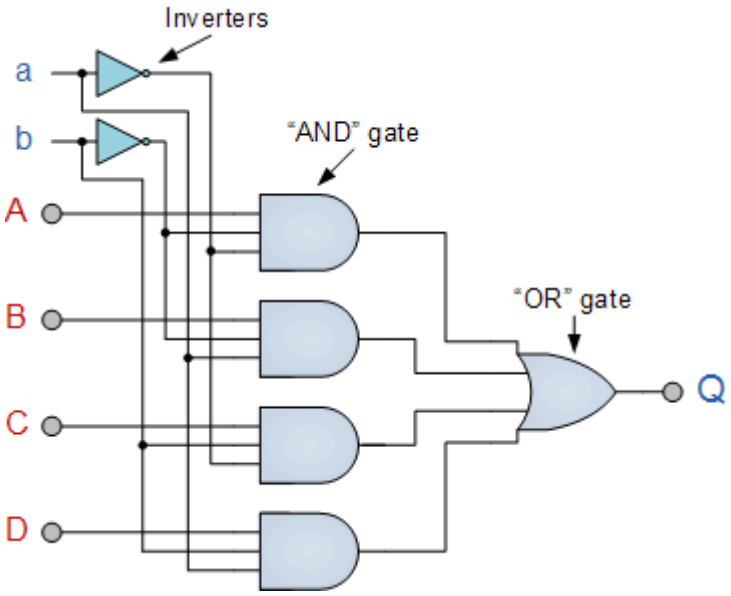


Figure 40 Multiplexer line selection

Adding more control address lines, (n) will allow the multiplexer to control more inputs as it can switch 2^n inputs but each control line configuration will connect only ONE input to the output.

Then the implementation of the Boolean expression above using individual logic gates would require the use of seven individual gates consisting of AND, OR and NOT gates as shown.

4 CHANNEL MULTIPLEXER USING LOGIC GATES



The symbol used in logic diagrams to identify a multiplexer is the following:

MULTIPLEXER SYMBOL

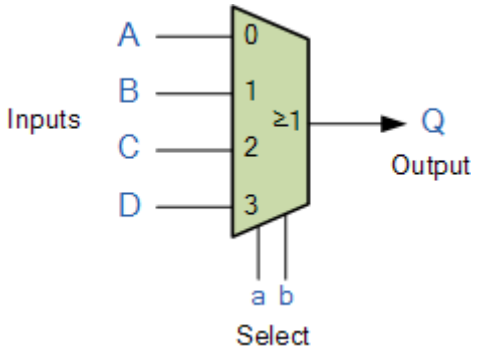


Figure 41 Schematic multiplexer symbol

Multiplexers are not limited to just switching a number of different input lines or channels to one common single output. There are also types that can switch their inputs to multiple outputs and have arrangements or 4-to-2, 8-to-3 or even 16-to-4 etc configurations and an example of a simple Dual channel 4 input multiplexer (4-to-2) is given below:

4-TO-2 CHANNEL MULTIPLEXER

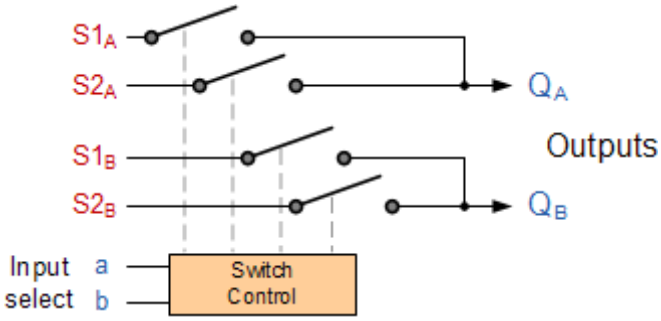


Figure 42 Multiple output multiplexer

Here in this example the 4 input channels are switched to 2 individual output lines but larger arrangements are also possible. This simple 4-to-2 configuration could be used for example, to switch audio signals for stereo pre-amplifiers or mixers.

ADJUSTABLE AMPLIFIER GAIN

As well as sending parallel data in a serial format down a single transmission line or connection, another possible use of multi-channel multiplexers is in digital audio applications as mixers or where the gain of an analogue amplifier can be controlled digitally, for example.

DIGITALLY ADJUSTABLE AMPLIFIER GAIN

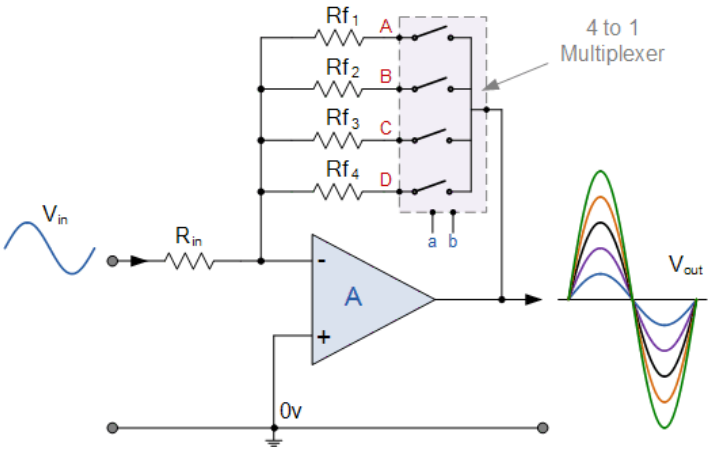


Figure 43 Adjustable gain multiplexer

A single 4-channel (Quad) SPST switch configured as a 4-to-1 channel multiplexer is connected in series with the resistors to select any feedback resistor to vary the value of Rf. The combination of these resistors will determine the overall gain of the amplifier, (Av). Then the gain of the amplifier can be adjusted digitally by simply selecting the appropriate resistor combination. Digital multiplexers are sometimes also referred to as "Data Selectors" as they select the data to be sent to the output line and are commonly used in communications or high speed network switching circuits such as LAN´s and Ethernet applications. Some multiplexer IC´s have a single inverting buffer (NOT Gate) connected to the output to give a positive logic output (logic "1", HIGH) on one terminal and a complimentary negative logic output (logic "0", LOW) on another different terminal.

It is possible to make simple multiplexer circuits from standard AND and OR gates as we have seen above, but commonly multiplexers/data selectors are available as standard i.c. packages such as the common TTL 74LS151 8-input to 1 line multiplexer or the TTL 74LS153 Dual 4-input to 1 line multiplexer. Multiplexer circuits with much higher number of inputs can be obtained by cascading together two or more smaller devices.

MULTIPLEXER SUMMARY

Then we can see that Multiplexers are switching circuits that just switch or route signals through themselves, and being a combinational circuit they are memoryless as there is no signal feedback path. The multiplexer is a very useful electronic circuit that has uses in many different applications such as signal routing, data communications and data bus control applications. When used with a demultiplexer, parallel data can be transmitted in serial form via a single data link such as a fiber-optic cable or telephone line and converted back into parallel data once again. The advantage is that only one serial data line is required instead of multiple parallel data lines. Therefore, multiplexers are sometimes referred to as "data selectors". Multiplexers can also be used to switch either analogue, digital or video signals, with the switching current in analogue power circuits limited to below 10mA to 20mA per channel in order to reduce heat dissipation.

For more check this page for a review of the multiplexer:

Useful link: http://www.electronics-tutorials.ws/combination/comb_2.html

COMBINATIONAL AND SEQUENTIAL LOGIC

INTRODUCTION

Combinational logic circuits implement Boolean functions. Boolean functions are mappings of input bitstrings to output bitstrings. These circuits are functions of input only.

What does that mean? It means that if you feed in an input to a circuit, say, 000, then look at its output, and discover it is, say, 10, then the output will always be 10 for that circuit, if 000 is the input. 000 is mapped to 10. If that value were not the same every single time, then the output must not completely depend on 000. Something else must be affecting the output. Combinational logic circuits always depend on input. Another way to define something that is a function of input is to imagine that you are only allowed to use input variables $x_{k-1},...,x_0$, i.e. data inputs, $c_{m-1},...,c_0$, i.e., control inputs, to write the function. This function can not depend on global variables or other variables.

EXAMPLE: COKE MACHINE

Let's consider a Coke machine to see if it is functional (i.e., behaves like a mathematical function). We want to see if its output is solely dependent on the input. Imagine this Coke machine only sells Coke, and that the price of a Coke is 75 cents. Furthemore, assume that it can only take quarters. Once 75 cents is deposited, a Coke is dispensed. You don't even have to press a button. You see this Coke machine, and think "I want a Coke", and you happen to be holding several quarters. You place the first quarter in the machine, and out comes...nothing! Undaunted, you put another quarter in, and out comes....nothing! Frustrated, you decide to put in yet another quarter, and out comes a Coke!

A mathematical function maps inputs to outputs. Thus, once you know what the input maps to, that should be it. In this case, the input (a quarter) mapped to nothing, nothing, and soda. So, clearly, this does not behave like a function. What's happening? Clearly, the machine is storing some information. In particular, it's records how much money you have entered so far. The output is determined not only by the input, but also by this stored information. This stored information is an example of state. State is basically internal information. Imagine, for example, that you have a linked list called **list**. You call **list.size()**. Does that method call always return the same value? The answer is no. The method call will return the current size of the linked list, which may change over time, as elements are added or removed from the list. Thus, the method is computing its value not only on the input (and there is none, since the **size()** method requires no arguments), but also based on the number of nodes in the object.

You can think of the data members as state. It is internal information recorded by the object. Any method does its computation based on the arguments passed in and based on the values of the data members.

SEQUENTIAL CIRCUITS

For this course, we represent states by a **k-bit** UB number. Given **k** bits, we can have up to 2^k different states.

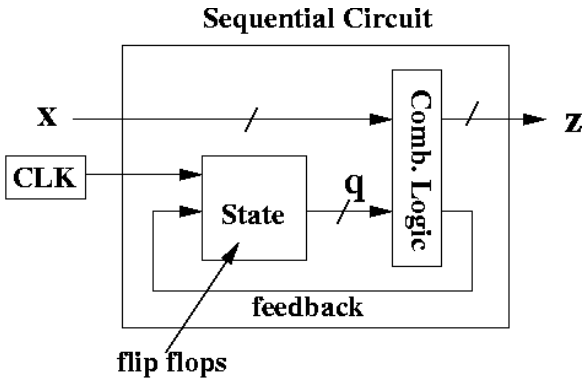


Figure 44 Sequencial circuit block diagram

Here are some of the key things to notice:

- Like combinational logic circuits, a sequential logic circuit has inputs (labelled with **x** with subscripts) and outputs (labelled with **z** with subscripts).
- Unlike combinational logic circuits, a sequential logic circuit uses a *clock*.
- Also, there is a box inside the circuit called **State**.
- This box contains flip flops. Assume it has **k** flip flops. The flip flops basically store a k-bit number representing the current state.
- The output **z** is computed based on the inputs (**x** with subscripts) and the state coming out of the state box (**q** with subscripts).
- The state may be updated at each positive clock edge. When there's not a positive clock edge, the state remains unchanged.
- The information needed to update to the state (called the *next state*) comes from the current state (the current value of **q**) and the input, which is fed through combinational logic, and fed back into the state box, telling the state box how to update itself.

For example, suppose you are currently in state 00, and see an input of 1. This may produce an output of, say, 10, and then produce feedback that tells the state box to update to state 01 by the next clock edge.

SUMMARY

A sequential circuit uses flip flops. Unlike combinational logic, sequential circuits have state, which means basically, sequential circuits have memory. The diagram shown earlier is one way to model sequential circuits. They can be modelled as finite state machines. We'll describe those in more detail in a future set of notes, so if you don't understand it, that's OK. It should be clearer in a future set of notes. The main difference between sequential circuits and combinational circuits is that sequential circuits compute their output based on input and state, and that the state is updated based on a clock. Combinational logic circuits implement Boolean functions, so they are functions only of their inputs, and are not based on clocks.

Useful link: https://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Seq/diff.html

HOW TO SIMPLIFY LOGIC NETWORKS

According to the theorems of boolean algebra it is usually possible to simplify a logic function describing a circuit, in order to simplify the circuit implementation aswell.

KARNAUGH MAP

Karnaugh Maps are used for many small design problems It's true that many larger designs are done using computer implementations of different algorithms. However designs with a small number of variables occur frequently in interface problems and that makes learning Karnaugh Maps worthwhile. In addition, if you study Karnaugh Maps you will gain a great deal of insight into digital logic circuits. In this section we'll examine some Karnaugh Maps for three and four variables. As we use them be particularly tuned in to how they are really being used to simplify Boolean functions. A Karnaugh Map is a grid-like representation of a truth table. It is really just another way of presenting a truth table, but the mode of presentation gives more insight. A Karnaugh map has zero and one entries at different positions. Each position in a grid corresponds to a truth table entry. The truth table is shown first. The Karnaugh Map for this truth table is shown after the truth table.

A	B	C	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

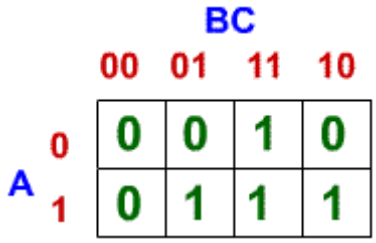


Figure 45 Karnaugh Map for the truth table above

At first, it might seem that the Karnaugh Map is just another way of presenting the information in a truth table. In one way that's true. However, any time you have the opportunity to use another way of looking at a problem advantages can accrue to you. In the case of the Karnaugh Map the advantage is that the Karnaugh Map is designed to present the information in a way that allows easy grouping of terms that can be combined.

Let's start by looking at the Karnaugh Map we've already encountered. Look at two entries side by side. We'll start by focussing on the ones shown below in gray.

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Let's examine the map again. The beauty of the Karnaugh Map is that it has been cleverly designed so that any two adjacent cells in the map differ by a change in one variable. It's always a change of one variable any time you cross a horizontal or vertical cell boundaries. (It's not fair to go through the corners!). Notice that the order of terms isn't random. Look across the top boundary of the Karnaugh Map. Terms go 00, 01, 11, 10. If you think binary well, you might have ordered terms in order 00, 01, 10, 11. That's the sequence of binary numbers for 0,1,2,3. However, in a Karnaugh Map terms are not arranged in numerical sequence! That's done deliberately to ensure that crossing each horizontal or vertical cell boundary will reflect a change of only one variable. In the numerical sequence, the middle two terms, 01, and 10 differ by two variables! Anyhow, when only one variable changes that means that you can eliminate that variable, as in the example above for the terms in the gray area. Let's check the claim made on above. Click on the buttons to shade groups of terms and to find out what the reduced term is. The Karnaugh Map is a visual technique that allows you to generate groupings of terms that can be combined with a simple visual inspection. The technique you use is simply to examine the Karnaugh Map for any groups of ones that occur. Grouping ones into the largest groups possible and ensuring that all ones in the table have been included are the first step in using a Karnaugh Map. In the next section we will examine how you can generate groups using Karnaugh Maps. First, however, we will look at some of the kinds of groups that occur in Truth Tables, and how they appear in Karnaugh Maps. There is a small surprise in one grouping above. The lower left and the lower right 1s actually form a group. They differ only in having B and its' inverse. Consequently they can be combined. You will have to imagine that the right end and the left end are connected. So far we have focussed on K-maps for three variables. Karnaugh Maps are useful for more than three variables, and we'll look at how to extend ideas to four variables here. Shown below is a K-map for four variables.

WX \ YZ	00	01	11	10
00	1	0	0	1
01	1	1	0	0
11	1	0	0	0
10	1	0	0	1

Figure 46 4-variables Karanugh map

Note the following facts about the four variable Karnaugh Map:

- There are 16 cells in the map. Anytime you have N variables, you will have 2^N possible combinations, and 2^N places in a truth table or Karnaugh Map.
- Imagine moving around in the Karnaugh Map. Every time you cross a horizontal or vertical boundary one - and only one - variable changes value.
- The two pairs of variables - WX and YZ - both change in the same pattern.

Otherwise, if you can understand a Karnaugh Map for a three-variable function, you should be able to understand one for a four-variable function. Remember these basic rules that apply to Karnaugh maps of any size.

- In a Karnaugh Map of any size, crossing a vertical or horizontal cell boundary is a change of only one variable - no matter how many variables there are.
- Each single cell that contains a 1 represents a minterm in the function, and each minterm can be thought of as a "product" term with N variables.
- To combine variables, use groups of 2, 4, 8, etc. A group of 2 in an N-variable Karnaugh map will give you a "product" term with N-1 variables. A group of 4 will have N-2 variables, etc.
- You will never have a group of 3, a group of 5, etc. Don't even think about it. See the points above.

EXAMPLE 1 - A GROUP OF 2

Here is a group of 2 in a 4-variable map.

WX \ YZ	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

Note that Y and Z are 00 and 01 at the top of the two columns in which you find the two 1s. The variable, Z, changes from a 0 to a 1 as you move from the left cell to the right cell. Consequently, these two 1s are not dependent upon the value of Z, and Z will not appear in the product term that results when we combine the 1s in this group of 2. Conversely, W, X and Y will be in the product term. Notice that in the row in which the 1s appear, W = 0 and X = 1. Also, in the two columns in which the 1s appear we have Y = 0. That means that the term represented by these two cells is:

$$\overline{W} \bullet X \bullet \overline{Y}$$

Larger groups in Karnaugh Maps of any size can lead to greater simplification. Let's consider the group shown shaded below. There are four terms covered by the shaded area.

WX \ YZ	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

- In the upper left:
  - $\overline{W} \bullet X \bullet \overline{Y} \bullet \overline{Z}$
- In the upper right;
  - $\overline{W} \bullet X \bullet Y \bullet \overline{Z}$
- In the lower left;
  - $W \bullet \overline{X} \bullet \overline{Y} \bullet \overline{Z}$
- In the lower right;
  - $W \bullet \overline{X} \bullet Y \bullet \overline{Z}$

These terms can be combined (assuming they are all ones in the Karnaugh Map!). The result is:

- By combining the first two terms above (the two terms at the top of the Karnaugh Map):
  - $\overline{W} \bullet X \bullet \overline{Z}$
- By combining the last two terms above (the two terms at the bottom of the Karnaugh Map):
  - $W \bullet \overline{X} \bullet \overline{Z}$
- Then, these two germs can be combined to give:
  - $X \bullet \overline{Z}$

Notice how making the grouping larger reduces the number of variables in the resulting terms. That simplification helps when you start to connect gates to implement the function represented by a Karnaugh map.

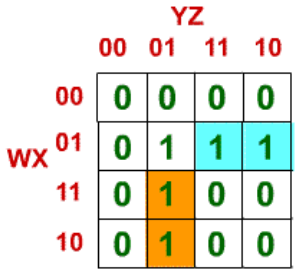
By now you should have inferred the rules for getting the sum-of-products form from the Karnaugh map.

- The number of ones in a group is a power of 2. That's 2, 4, 8 etc.
- If a variable takes on both values (0 and 1) for different entries (1s) in the Karnaugh Map, that variable will not be in the sum-of-products form. Note that the variable should be one in half of the K-Map ones and it should be zero (inverted) in the other half.
- If a variable is always 1 or always zero (it appears either inverted all the time in all entries that are one, or it is always not inverted) then that variable appears in that form in the sum-of-products form.

Some Further Observations

There are a few further observations that should be made. Note the following:

- There may well be more than one solution of equal complexity.
    - Here is an example Karnaugh Map. There are two groups that are obvious - one in orange, and one in light blue.



    - In this example, the two terms shown are:
    - There is still one entry to account for. There is a 1 that can be joined to either of two other entries to form a group. There is no best way to go on this. Either way will take the same number of gates, inputs, etc.

And another observation

- If there are more than four variables, it is still possible to use Karnaugh Maps, and you will find larger Karnaugh Maps discussed in many textbooks. However, as the number of variables increases it becomes more difficult to see patterns, and computer methods start to become more attractive.

For more and for examples take a look at Karnaugh map on this page:

Useful link: https://www.facstaff.bucknell.edu/mastascu/eLessonsHTML/Logic/Logic3.html

ELECTROMAGNETIC FIELDS

INTUITIVE INTRODUCTION TO MAXWELL EQUATIONS:

Maxwell's Equations are a set of 4 complicated equations that describe the world of electromagnetics. These equations describe how electric and magnetic fields propagate, interact, and how they are influenced by objects. James Clerk Maxwell [1831-1879] was an Einstein/Newton-level genius who took a set of known experimental laws (Faraday's Law, Ampere's Law) and unified them into a symmetric coherent set of Equations known as Maxwell's Equations. Maxwell was one of the first to determine the speed of propagation of electromagnetic (EM) waves was the same as the speed of light - and hence to conclude that EM waves and visible light were really the same thing. Maxwell's Equations are critical in understanding Antennas and Electromagnetics. They are formidable to look at - so complicated that most electrical engineers and physicists don't even really know what they mean. Shrouded in complex math (which is likely so "intellectual" people can feel superior in discussing them), true understanding of these equations is hard to come by. This leads to the reason for this website - an intuitive tutorial of Maxwell's Equations. I will avoid if at all possible the mathematical difficulties that arise, and instead describe what the equations mean. And don't be afraid - the math is so complicated that those who do understand complex vector calculus still cannot apply Maxwell's Equations in anything but the simplest scenarios. For this reason, intuitive knowledge of Maxwell's Equations is far superior than mathematical manipulation-based knowledge. To understand the world, you must understand what equations mean, and not just know mathematical constructs. I believe the accepted methods of teaching electromagnetics and Maxwell's Equations do not produce understanding. And with that, let's say something about these equations. Maxwell's Equations are laws - just like the law of gravity. These equations are rules the universe uses to govern the behavior of electric and magnetic fields. A flow of electric current will produce a magnetic field. If the current flow varies with time (as in any wave or periodic signal), the magnetic field will also give rise to an electric field. Maxwell's Equations shows that separated charge (positive and negative) gives rise to an electric field - and if this is varying in time as well will give rise to a propagating electric field, further giving rise to a propgating magnetic field. To understand Maxwell's Equations at a more intuitive level than most Ph.Ds in Engineering or Physics, click through the links and definitions above. You'll find that the complicated math masks an inner elegance to these equations - and you'll learn how the universe operates the Electromagnetic Machine.

1. $\nabla \cdot \mathbf{D} = \rho_V$
2. $\nabla \cdot \mathbf{B} = 0$
3. $\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$
4. $\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J}$

GAUSS' LAW FOR ELECTRIC FIELDS

GAUSS' LAW

Gauss' Law is the first of Maxwell's Equations which dictates how the Electric Field behaves around electric charges. Gauss' Law can be written in terms of the Electric Flux Density and the Electric Charge Density as:

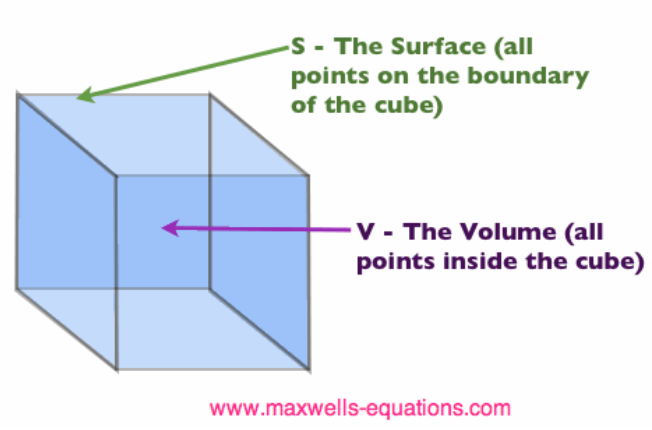
$$\nabla \cdot \mathbf{D} = \rho_V$$

The symbol $\nabla \cdot$ is the divergence operator. The equation is known as Gauss' Law in point form. That is, the equation is true at any point in space. That is, if there exists electric charge somewhere, then the divergence of **D** at that point is nonzero, otherwise it is equal to zero. To get some more intuition on Gauss' Law, let's look at Gauss' Law in integral form. To do this, we assume some arbitrary volume (we'll call it *V*) which has a boundary (which is written *S*). Then integrating the differential equation over the volume *V* gives Gauss' Law in integral form:

$$\int_V (\nabla \cdot \mathbf{D}) dV = \int_V \rho_V dV$$

$$\Rightarrow \quad \int_S \mathbf{D} \cdot \mathbf{dS} = Q_{enc}$$

I probably made things less clear, but let's go through it real quick. As an example, look at the following figure. We have a volume *V*, which is the cube. The surface *S* is the boundary of the cube (i.e. the 6 flat faces that form the boundary of the volume).



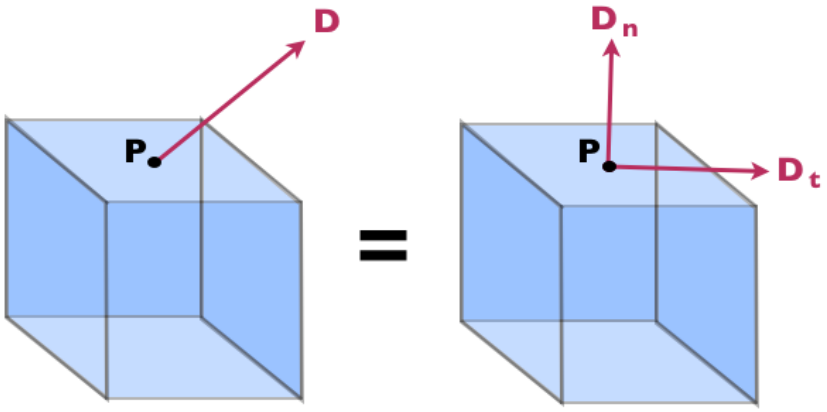
The integral equation states that the amount of charge inside a volume *V* (= Q_{enc}) is equal to the total amount of Electric Flux (**D**) exiting the surface *S*. That is, to determine the Electric Flux leaving the region *V*, we only need to know how much electric charge is within the volume.

We rewrite the last equation:

$\mathbf{D} \cdot \mathbf{dS}$ = This means we are only interested in the component of **D** that is entering or exiting the volume V. We don't care about "the tangential" components of **D** - these circle around the volume but don't contribute to the net Electric Flux in or out of the volume.

$\int_S \mathbf{D} \cdot \mathbf{dS}$ = This means we want to sum up the $\mathbf{D} \cdot \mathbf{dS}$ values at each point along the surface *S*.

An example with the cube in figure might help make this clear. Look at the point *P* in Figure, where we have drawn the **D** field vector:



We can rewrite any field in terms of its tangential and normal components, as shown in Figure. From the last equation, we are only interested in the component of **D** normal (orthogonal or perpendicular) to the surface *S*. We write this as **Dn**. The tangential component **Dt** flows along the surface. If you imagine the **D** field as a water flow, then only the component **Dn** would contribute to water leaving the volume - **Dt** is just water flowing around the surface. Hence, Gauss' law is a mathematical statement that the total Electric Flux exiting any volume is equal to the total charge inside. Hence, if the volume in question has no charge within it, the net flow of Electric Flux out of that region is zero. If there is positive charge within a volume, then there exists a positive amount of Electric Flux exiting any volume that surrounds the charge. If there is negative charge within a volume, then there exists a negative amount of Electric Flux exiting (i.e. the Electric Flux enters the volume).

INTERPRETATION OF GAUSS' LAW

What does this matter? Gauss' Law states that electric charge acts as sources or sinks for Electric Fields. If you use the water analogy again, positive charge gives rise to flow out of a volume - this means positive electric charge is like a source (a faucet - pumping water into a region). Conversely, negative charge gives rise to flow into a volume - this means negative charge acts like a sink (fields

flow into a region and terminate on the charge). This gives us a lot of intuition about the way fields can physically act in any scenario. For instance, here are possible and impossible situations for the Electric Field, as decided by the universe in the Law of Gauss it setup:

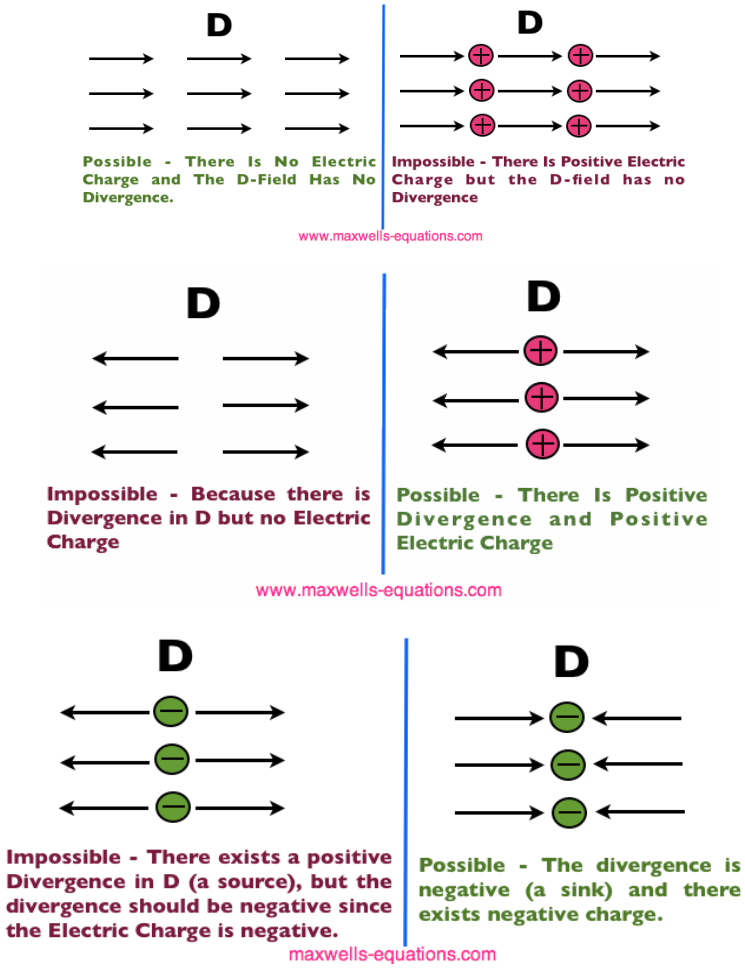


Figure 47 Some possible-vs-impossible situations for electric fields

If you observe the way the D field must behave around charge, you may notice that Gauss' Law then is equivalent to the Force Equation for charges, which gives rise to the E field equation for point charges:

$$F = \frac{q_1 q_2}{4\pi\varepsilon_0 R^2}$$

$$|\mathbf{E}| = \frac{q}{4\pi\varepsilon_0 R^2}$$

$$|\mathbf{D}| = \frac{q}{4\pi R^2}$$

The above equations shows that charges exert a force on them, which means there exists E-fields that are away from positive charge and towards negative charge. This means opposite charges attract and negative charges repel. And since **D** and **E** are related by permittivity, we see that Gauss' Law is a more formal statement of the force equation for electric charges.

In summary, Gauss' Law means the following is true:

- **D** and **E** field lines diverge away from positive charges
- **D** and **E** field lines diverge towards negative charges
- **D** and **E** field lines start and stop on Electric Charges
- Opposite charges attract and negative charges repel
- The divergence of the **D** field over any region (volume) of space is exactly equal to the net amount of charge in that region.

GAUSS' LAW FOR MAGNETIC FIELDS

Before you read this page, you should have read the page on Gauss' Law for Electric Fields. If that makes sense, then the second of Maxwell's Equations will be pretty easy. First, observe both of Gauss' Laws, written as:

$$\nabla \cdot \mathbf{D} = \rho_V$$
$$\nabla \cdot \mathbf{B} = 0$$

You see that both of these equations specify the divergence of the field in question. For the top equation, we know that Gauss' Law for Electric Fields states that the divergence of the Electric Flux Density **D** is equal to the volume electric charge density. But the second equation, Gauss' Magnetism law states that the divergence of the Magnetic Flux Density (**B**) is zero. Why isn't the divergence of **B** equal to the *magnetic charge density*? Well - it is. But it just so happens that no one has ever found magnetic charge - not in a laboratory or on the street or on the subway. And therefore, until this hypothetical magnetic charge is found, we set the right side of Gauss' Law for Magnetic Fields to zero:

Gauss' Law For Magnetism

$\nabla \cdot \mathbf{B} = 0$ (Magnetic Charge Does Not Exist)

$\nabla \cdot \mathbf{H} = 0$ (also true since $\mathbf{B} = \mu\mathbf{H}$)

Since **B** and the Magnetic Field **H** are related by the permeability μ, we note that the divergence of the magnetic field is also zero.

Now, you may have played with magnets when you were little, and these magnetic objects attracted other magnets similar to how electric charges repel or attract like electric charges. However, there is something special about these magnets - they always have a positive and negative end. This means every magnetic object is a magnetic dipole, with a north and south pole. No matter how many times you break the magnetic in half, it will just form more magnetic dipoles. Gauss' Law for Magnetism states that magnetic monopoles do not exist - or at least we haven't found them yet. Because we know that the divergence of the Magnetic Flux Density is always zero, we now know a little bit

about how these fields behave. I'll present a couple of examples of legal and illegal Magnetic Fields, which are a consequence of Gauss' Law for Magnetism:

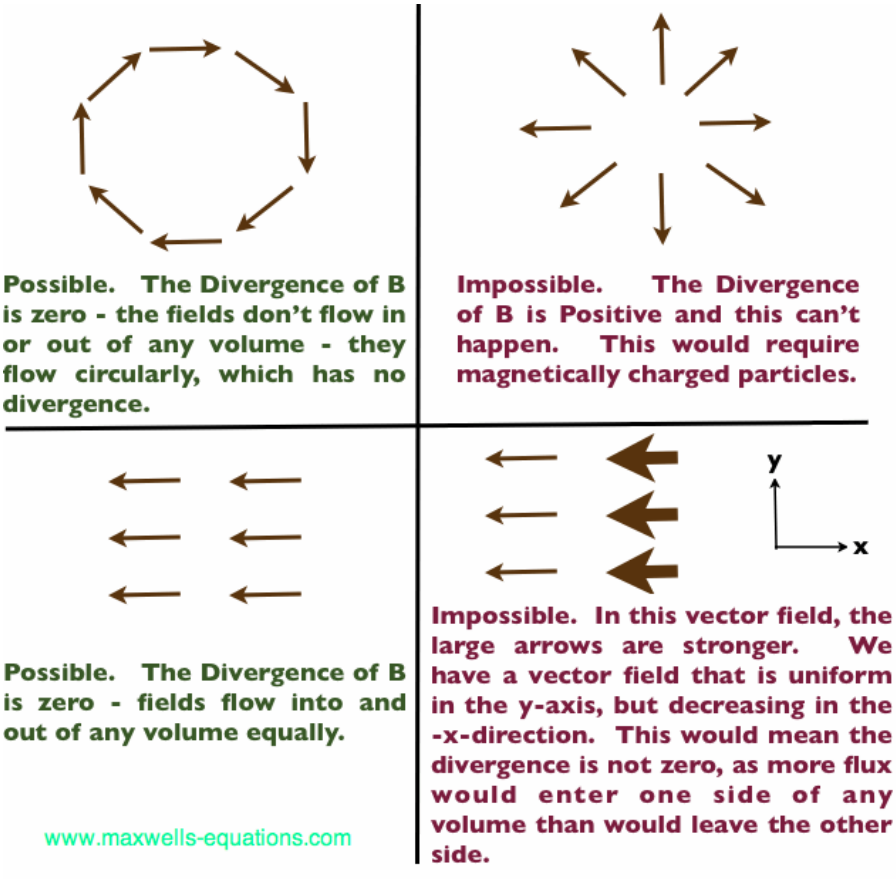


Figure 48 Some possible-vs-impossible magnetic fields

In summary, the second of Maxwell's Equations - Gauss' Law For Magnetism - means that:

- Magnetic Monopoles Do Not Exist
- The Divergence of the **B** or **H** Fields is Always Zero Through Any Volume
- Away from Magnetic Dipoles, Magnetic Fields flow in a closed loop. This is true even for plane waves, which just so happen to have an infinite radius loop.

There you have it - Gauss' Law for Magnetic Fields. If you understood Gauss' Law for Electric Fields, this isn't very complicated.

FARADAY'S LAW

Here we'll explain the meaning of the 3rd of Maxwell's Equations, **Faraday's Law**, which is given by

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$$

Faraday was a scientist experimenting with circuits and magnetic coils way back in the 1830s. His experiment setup, which led to Farday's Law, is shown below:

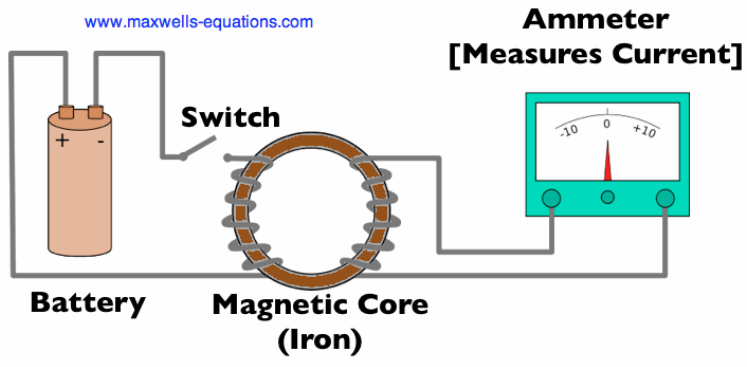


Figure 49 Faraday's experiment

The experiment itself is somewhat simple. When the battery is disconnected, we have no electric current flowing through the wire. Hence there is no magnetic flux induced within the Iron (Magnetic Core). The Iron is like a highway for Magnetic Fields - they flow very easily through magnetic material. So the purpose of the core is to create a path for the Magnetic Flux to flow. When the switch is closed, the electric current will flow within the wire attached to the battery. When this current flows, it has an associated magnetic field (or magnetic flux) with it. When the wire wraps around the left side of the magnetic core (as shown in Figure 1), a magnetic field (magnetic flux) is induced within the core. This flux travels around the core. So the Magnetic Flux produced by the wired coil on the left exists within the wired coil on the right, which is connected to the ammeter. Now, a funny thing happens, which Faraday observed. When he closed the switch, then current would begin flowing and the ammeter would spike one way (say measuring +10 Amps on the other side). But this was very brief, and the current on the right coil would go to zero. When the switch was opened, the measured current would spike to the other side (say -10 Amps would be measured), and then the measured current on the right side would again be zero.

Faraday figured out what was happening. When the switch was initially changed from open to closed, the magnetic flux within the magnetic core increased from zero to some maximum number (which was a constant value, versus time). When the flux was increasing, there existed an induced current on the opposite side. Similarly, when the switch was opened, the magnetic flux in the core would decrease from it's constant value back to zero. Hence, a decreasing flux within the core induced an opposite current on the right side. Faraday figured out that a changing Magnetic Flux within a circuit (or closed loop of wire) produced an induced *EMF*, or voltage within the circuit.

He wrote this as:

$$EMF = -\frac{d\Phi}{dt}$$

In this equation, Φ is the Magnetic Flux within a circuit, and *EMF* is the electro-motive force, which is basically a voltage source. The last equation then says that the induced voltage in a circuit is the opposite of the time-rate-of-change of the magnetic flux. This equation is known as *Lenz's Law*. Lenz was the guy who figured out the minus sign. *We know that an electric current gives rise to a magnetic field - but thanks to Faraday we also know that a magnetic field within a loop gives rise to an electric current.* The universe loves symmetry and Maxwell's Equations has a lot of it.

DERIVING FARADAY'S LAW

Now, we have the experimental result of the last equation, how do we go from this result to the standard form of Farday's Law? Let's imagine a simple loop, with a time varying **B** field within it:

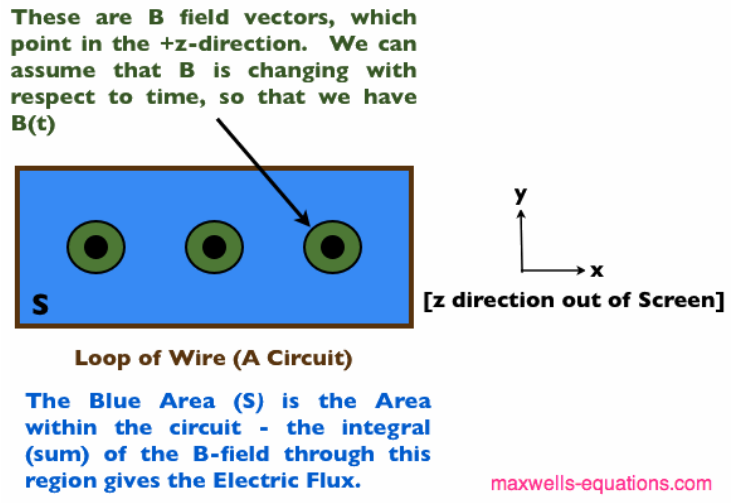


Figure 50 Faraday's law experiment

We know that the rate of change of the total magnetic flux is equal to the opposite of the *EMF*, or the electric force within the wire.

The total magnetic flux is simply the integral (or sum) of the **B** field over the area enclosed by the wire:

$$\Phi(t) = \int_S \mathbf{B}(t)\, d\mathbf{S}$$ [The Magnetic Flux Φ is the Sum (Average) of the **B** – field over the area S]

To find the total *EMF* induced around the whole circuit, we sum up over the length of the wire the *EMF* produced at each point. This is known as a line integral.

This is written as:

$$EMF_{total} = \oint_{Circuit} d(EMF)$$ [the total EMF around the circuit is equal to summing up the small contributions at each point $d(EMF)$ around the entire circuit]

Now, recall that the Electric Field is directly related to force from electric charges. And Voltage is also defined as the sum (integral) of the Electric Field across a path [recall that the E-field is measured in Volts/meter]. Hence, the E-field is actually the spatial-derivative of voltage (E-field is equal to the rate of change of the voltage with respect to distance). These facts are summed up in the following:

$$V = \int \mathbf{E} \cdot d\mathbf{l}$$ [voltage between two points is the sum of the E-field along the path between the points]

$$\mathbf{E} = \frac{dV}{dl}$$ [the E-field is a measure of how fast the Voltage is Changing Along a Path]

Hence, these equations tell us that the differential amount of *EMF* at any point along the circuit is equal to the **E** field at that location. Therefore:

$$EMF_{total} = \oint_{Circuit} \mathbf{E} \cdot \mathbf{dL}$$ [the total EMF around the circuit is equal to summing up **E** field around the length of the circuit]

Now, some mathematician named Stokes figured out that integrating (averaging) of a field around a loop is exactly equivalent to integrating the curl of the field within the loop. This should have somewhat of an intuitive truth to you: the curl is the measure of the rotation of a field, so the curl of a vector field within a surface should be related to the integral of a field around a loop that encloses the surface.

$$\oint_{Circuit} \mathbf{E} \cdot \mathbf{dL} = \int_{S} \nabla \times \mathbf{E} \cdot \mathbf{dS}$$ [Stokes' Theorem]

Now we are almost there. By replacing the various terms we get:

$$EMF = -\frac{d\Phi}{dt}$$

$$\int_S \nabla \times \mathbf{E} \cdot \mathbf{dS} = -\frac{d}{dt}\int_S \mathbf{B}(t) \cdot \mathbf{dS} = \int_S \frac{-d\mathbf{B}(t)}{dt} \cdot \mathbf{dS}$$

$$\Rightarrow \nabla \times \mathbf{E} = \frac{-\partial \mathbf{B}(t)}{\partial t}$$

In the last equation we note that if we have two integrals over surfaces, and the surfaces can be however we choose, then the quantities we integrate must also be the same.

Interpretation of Farday's Law

Faraday's law shows that a changing magnetic field within a loop gives rise to an induced current, which is due to a force or voltage within that circuit. We can then say the following about Farday's Law:

- Electric Current gives rise to magnetic fields. Magnetic Fields around a circuit gives rise to electric current.
- A Magnetic Field Changing in Time gives rise to an E-field circulating around it.
- A circulating E-field in time gives rise to a Magnetic Field Changing in time.

Farday's Law is very powerful as it shows how much the universe loves symmetry. If a current gives rise to a Magnetic Field then a Magnetic Field can give rise to an electric current. And a changing E-field in space gives rise to a changing B-field in time.

Ampere's Law

Here, we'll explain the meaning of the last of Maxwell's Equations, **Ampere's Law**, which is given by:

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J}$$

I'm going to start by presenting Ampere's Law, which relates a electric current flowing and a magnetic field wrapping around it:

$$\oint \mathbf{H} \cdot \mathbf{dL} = I_{enc}$$

This equation can be explained: suppose you have a conductor (wire) carrying a current, *I*. Then this current produces a Magnetic Field which circles the wire. The left side of it means: if you take any imaginary path that encircles the wire, and you add up the Magnetic Field at each point along that path, then it will numerically equal the amount of current that is encircled by this path (which is why we write I_{enc} for encircled or enclosed current).

EXAMPLE

Suppose we have a long wire carrying a constant electric current, *I* [Amps]. What is the magnetic field around the wire, for any distance *r* [meters] from the wire?

Let's look at the diagram in Figure. We have a long wire carrying a current of *I* Amps. We want to know what the Magnetic Field is at a distance *r* from the wire. So we draw an imaginary path around the wire, which is the dotted blue line on the right in Figure:

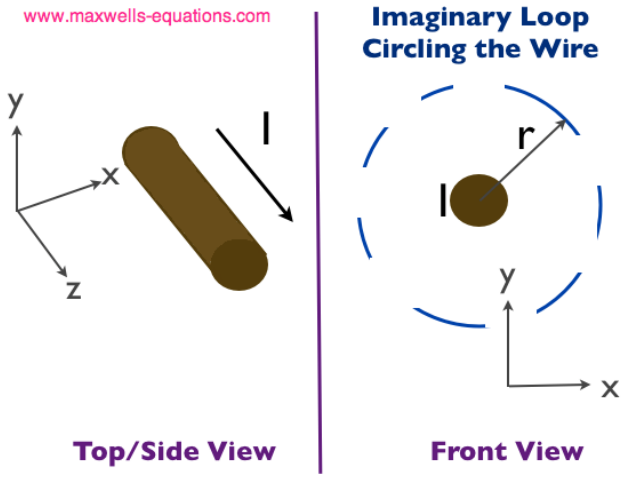


Figure 51 Magnetic field in a conductive wire

Ampere's Law states that if we add up (integrate) the Magnetic Field along this blue path, then numerically this should be equal to the enclosed current *I*. Now, due to symmetry, the magnetic field will be uniform (not varying) at a distance *r* from the wire. The path length of the blue path in Figure is equal to the circumference of a circle of radius *r*: $2\pi r$.

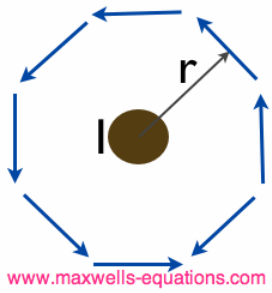
If we are adding up a constant value for the magnetic field (we'll call it *H*), then the left side becomes simple:

$$\oint \mathbf{H} \cdot \mathbf{dL} = 2\pi r H = I_{enc}$$

$$\Rightarrow H = \frac{I_{enc}}{2\pi r}$$

Hence, we have figured out what the magnitude of the **H** field is. And since *r* was arbitrary, we know what the H-field is everywhere. The last states that the Magnetic Field decreases in magnitude as you move farther from the wire (due to the 1/r term). So we've used Ampere's Law to find the magnitude of the Magnetic Field around a wire. However, the **H** field is a Vector Field, which means at every location is has both a magnitude and a direction. The direction of the H-field is everywhere tangential to the imaginary loops, as shown in Figure. The right hand rule determines the sense of direction of the magnetic field:

$$\mathbf{H} = \frac{I_{enc}}{2\pi r}$$



MANIPULATING THE MATH FOR AMPERE'S LAW

We are going to do the same trick with Stoke's Theorem that we did when looking at Faraday's Law. We can rewrite Ampere's Law as:

$$I_{enc} = \oint \mathbf{H} \cdot \mathbf{dL} = \int_S (\nabla \times \mathbf{H}) \cdot d\mathbf{S}$$

On the right side equality we have used Stokes' Theorem to change a line integral around a closed loop into the curl of the same field through the surface enclosed by the loop (S).

We can also rewrite the total current I_{enc} as the surface integral of the Current Density (**J**):

$$I_{enc} = \int_S \mathbf{J} \cdot \mathbf{dS}$$

So now we have the original Ampere's Law rewritten in terms of surface integrals (two last equations). Hence, we can substitute them together and get a new form for Ampere's Law:

$$\int_S (\nabla \times \mathbf{H}) \cdot d\mathbf{S} = \int_S \mathbf{J} \cdot d\mathbf{S}$$

$$\Rightarrow \quad \nabla \times \mathbf{H} = \mathbf{J}$$

Now, we have a new form of Ampere's Law: the curl of the magnetic field is equal to the Electric Current Density.

DISPLACEMENT CURRENT DENSITY

Ampere's Law was written as in the last form up until Maxwell. So let's look at what is wrong with it. First, I have to throw out another vector identity - the divergence of the curl of any vector field is always zero:

$$\nabla \cdot (\nabla \times \mathbf{H}) = 0 \quad \text{[This is true for any vector field]}$$

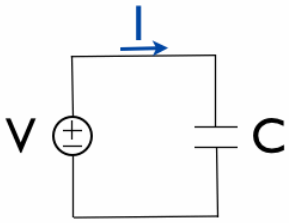
"Divergence of the Curl is Zero"

So let's take the divergence of Ampere's Law:

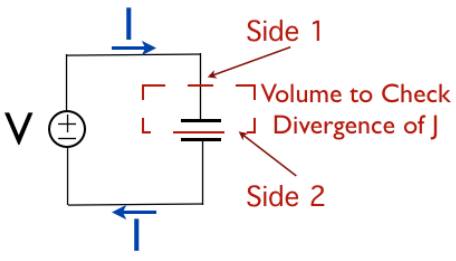
$$\nabla \times \mathbf{H} = \mathbf{J}$$
$$\nabla \cdot (\nabla \times \mathbf{H}) = \nabla \cdot \mathbf{J}$$
$$0 = \nabla \cdot \mathbf{J} \quad \text{[the divergence of J is always zero?]}$$

This equation states that the divergence of the current density **J** is always zero. Is this true?

If the divergence of **J** is always zero, this means that the electric current flowing into any region is always equal to the electric current flowing out of the region (no divergence). This seems somewhat reasonable, as electric current in circuits flows in a loop. But let's look what happens if we put a capacitor in the circuit:



Now, we know from electric circuit theory that if the voltage is not constant then current will flow through the capacitor. That is, we have **I** not equal to zero in Figure. However, a capacitor is basically two parallel conductive plates separated by air. Hence, there is no conductive path for the current to flow through. This means that no electric current can flow through the air of the capacitor. To show it more clearly, let's take a volume that goes through the capacitor, and see if the divergence of **J** is zero:



In Figure, we have drawn an imaginary volume in red, and we want to check if the divergence of the current density is zero. The volume we've chosen, has one end (labeled side 1) where the current enters the volume via the black wire. The other end of our volume (labeled side 2) splits the capacitor in half. We know that the current flows in the loop. So current enters through Side 1 of our red volume. However, there is no electric current that exits side 2. No current flows within the air of the capacitor. This means that current enters the volume, but nothing leaves it - so the divergence of **J** is not zero. We have just violated our equation which means the theory does not hold. And this was the state of things, until our friend Maxwell came along. Maxwell knew that the Electric Field (and Electric Flux Density (D) was changing within the capacitor. And he knew that a time-varying magnetic field gave rise to a solenoidal Electric Field (i.e. this is Farday's Law - the curl of E equals the time derivative of B). So, why is not that a time varying D field would give rise to a solenoidal H field (i.e. gives rise to the curl of H). The universe loves symmetry, so why not introduce this term? And so Maxwell did, and he called this term the displacement current density:

$$\frac{\partial \mathbf{D}}{\partial t} = \mathbf{J}_d \quad \text{[Displacement Current Density]}$$

This term would "fix" the circuit problem we have and would make Farday's Law and Ampere's Law more symmetric. This was Maxwell's great contribution. And you might think it is a weak contribution. But the existence of this term unified the equations and led to understanding the propagation of electromagnetic waves, and the proof that all waves travel at the same speed (the speed of light)! And it was this unification of the equations that Maxwell presented, that led the collective set to be known as Maxwell's Equations. So, if we add the displacement current to Ampere's Law, then we have the final form of Ampere's Law:

$$\nabla \times \mathbf{H} = \mathbf{J} + \mathbf{J}_d$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}$$

INTREPRETATION OF AMPERE'S LAW

So what does the last equation mean? The following are consequences of this law:

- A flowing electric current (**J**) gives rise to a Magnetic Field that circles the current
- A time-changing Electric Flux Density (**D**) gives rise to a Magnetic Field that circles the **D** field

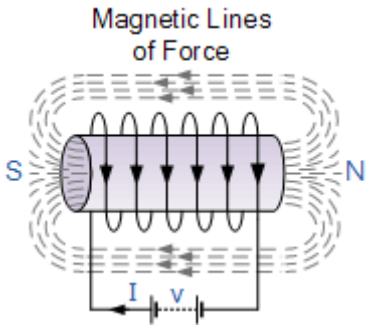
Ampere's Law with the contribution of Maxwell nailed down the basis for Electromagnetics as we currently understand it. And so we know that a time varying **D** gives rise to an **H** field, but from Farday's Law we know that a varying **H** field gives rise to an **E** field.... and so on and so forth and the electromagnetic waves propagate.

For more check the website

Useful link: http://www.maxwells-equations.com/

ELECTROMAGNETIC INDUCTION:

If the wire is then wound into a coil, the magnetic field is greatly intensified producing a static magnetic field around itself forming the shape of a bar magnet giving a distinct North and South pole.

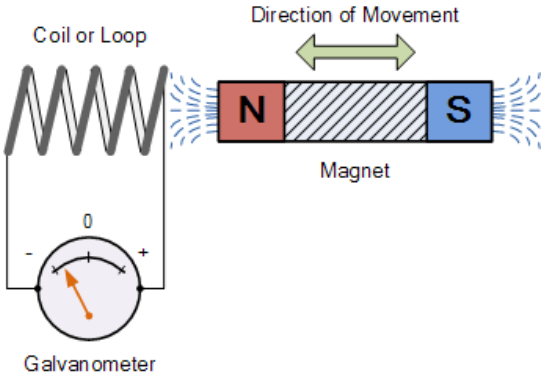


The magnetic flux developed around the coil being proportional to the amount of current flowing in the coils windings as shown. If additional layers of wire are wound upon the same coil with the same current flowing through them, the static magnetic field strength would be increased. Therefore, the magnetic field strength of a coil is determined by the *ampere turns* of the coil. With more turns of wire within the coil, the greater the strength of the static magnetic field around it. But what if we reversed this idea by disconnecting the electrical current from the coil and instead of a hollow core we placed a bar magnet inside the core of the coil of wire. By moving this bar magnet "in" and "out" of the coil a current would be induced into the coil by the physical movement of the magnetic flux inside it. Likewise, if we kept the bar magnet stationary and moved the coil back and forth within the magnetic field an electric current would be induced in the coil. Then by either moving the wire or changing the magnetic field we can induce a voltage and current within the coil and this process is known as Electromagnetic Induction and is the basic principal of operation of transformers, motors and generators.

Electromagnetic Induction was first discovered way back in the 1830's by Michael Faraday. Faraday noticed that when he moved a permanent magnet in and out of a coil or a single loop of wire it induced an ElectroMotive Force or emf, in other words a Voltage, and therefore a current was produced. So what Michael Faraday discovered was a way of producing an electrical current in a circuit by using only the force of a magnetic field and not batteries. This then lead to a very important law linking electricity with magnetism, Faraday's Law of Electromagnetic Induction. So how does this work?.

When the magnet shown below is moved "towards" the coil, the pointer or needle of the Galvanometer, which is basically a very sensitive centre zero'ed moving-coil ammeter, will deflect away from its centre position in one direction only. When the magnet stops moving and is held stationary with regards to the coil the needle of the galvanometer returns back to zero as there is no physical movement of the magnetic field. Likewise, when the magnet is moved "away" from the coil in the other direction, the needle of the galvanometer deflects in the opposite direction with regards to the first indicating a change in polarity. Then by moving the magnet back and forth towards the coil the needle of the galvanometer will deflect left or right, positive or negative, relative to the directional motion of the magnet.

ELECTROMAGNETIC INDUCTION BY A MOVING MAGNET



Likewise, if the magnet is now held stationary and ONLY the coil is moved towards or away from the magnet the needle of the galvanometer will also deflect in either direction. Then the action of moving a coil or loop of wire through a magnetic field induces a voltage in the coil with the magnitude of this induced voltage being proportional to the speed or velocity of the movement. Then we can see that the faster the movement of the magnetic field the greater will be the induced emf or voltage in the coil, so for Faraday's law to hold true there must be "relative motion" or movement between the coil and the magnetic field and either the magnetic field, the coil or both can move.

FARADAY'S LAW OF INDUCTION

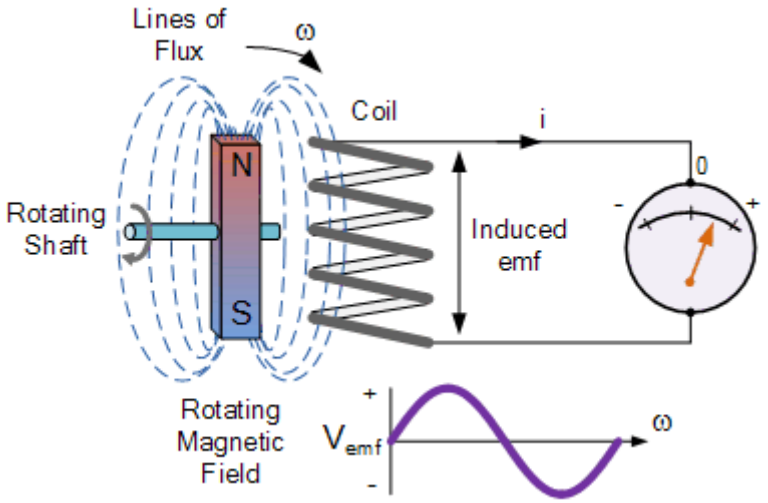
From the above description we can say that a relationship exists between an electrical voltage and a changing magnetic field to which Michael Faraday's famous law of electromagnetic induction states: "that a voltage is induced in a circuit whenever relative motion exists between a conductor and a magnetic field and that the magnitude of this voltage is proportional to the rate of change of the flux". In other words, Electromagnetic Induction is the process of using magnetic fields to produce voltage, and in a closed circuit, a current.
So how much voltage (emf) can be induced into the coil using just magnetism. Well this is determined by the following 3 different factors.

- Increasing the number of turns of wire in the coil – By increasing the amount of individual conductors cutting through the magnetic field, the amount of induced emf produced will be the sum of all the individual loops of the coil, so if there are 20 turns in the coil there will be 20 times more induced emf than in one piece of wire.
- Increasing the speed of the relative motion between the coil and the magnet – If the same coil of wire passed through the same magnetic field but its speed or velocity is increased, the wire will cut the lines of flux at a faster rate so more induced emf would be produced.
- Increasing the strength of the magnetic field – If the same coil of wire is moved at the same speed through a stronger magnetic field, there will be more emf produced because there are more lines of force to cut.

If we were able to move the magnet in the diagram above in and out of the coil at a constant speed and distance without stopping we would generate a continuously induced voltage that would alternate between one positive polarity and a negative polarity producing an alternating or AC output voltage and this is the basic principal of how a Generator works similar to those used in dynamos and car alternators.

In small generators such as a bicycle dynamo, a small permanent magnet is rotated by the action of the bicycle wheel inside a fixed coil. Alternatively, an electromagnet powered by a fixed DC voltage can be made to rotate inside a fixed coil, such as in large power generators producing in both cases an alternating current.

Simple Generator using Magnetic Induction



The simple dynamo type generator above consists of a permanent magnet which rotates around a central shaft with a coil of wire placed next to this rotating magnetic field. As the magnet spins, the magnetic field around the top and bottom of the coil constantly changes between a north and a south pole. This rotational movement of the magnetic field results in an alternating emf being induced into the coil as defined by Faraday's law of electromagnetic induction. The magnitude of the electromagnetic induction is directly proportional to the flux density, β the number of loops giving a total length of the conductor, l in meters and the rate or velocity, v at which the magnetic field changes within the conductor in meters/second or m/s, giving by the motional emf expression:

Faraday's Motional emf Expression

$$\mathcal{E} = -\beta.\ell.\upsilon \quad \text{volts}$$

If the conductor does not move at right angles (90°) to the magnetic field then the angle θ° will be added to the above expression giving a reduced output as the angle increases:

$$\mathcal{E} = -\beta.\ell.\upsilon \sin\theta \quad \text{volts}$$

Lenz's Law of Electromagnetic Induction

Faraday's Law tells us that inducing a voltage into a conductor can be done by either passing it through a magnetic field, or by moving the magnetic field past the conductor and that if this conductor is part of a closed circuit, an electric current will flow. This voltage is called an induced emf as it has been induced into the conductor by a changing magnetic field due to electromagnetic induction with the negative sign in Faraday's law telling us the direction of the induced current (or polarity of the induced emf).

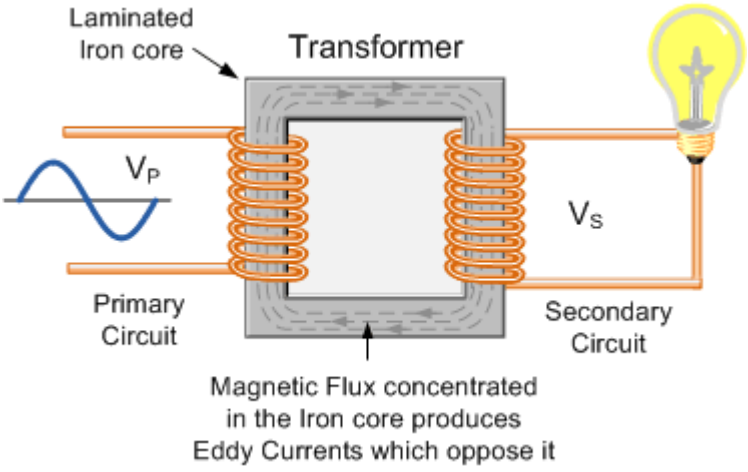
But a changing magnetic flux produces a varying current through the coil which itself will produce its own magnetic field as we saw in the Electromagnets tutorial. This self-induced emf opposes the change that is causing it and the faster the rate of change of current the greater is the opposing emf. This self-induced emf will, by Lenz's law oppose the change in current in the coil and because of its direction this self-induced emf is generally called a back-emf.

Lenz's Law states that:" the direction of an induced emf is such that it will always opposes the change that is causing it". In other words, an induced current will always OPPOSE the motion or change which started the induced current in the first place and this idea is found in the analysis of Inductance.

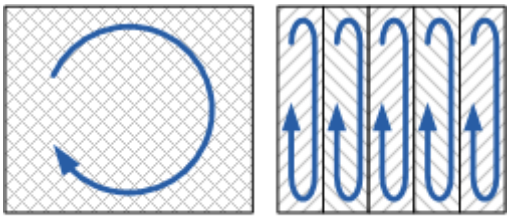
Likewise, if the magnetic flux is decreased then the induced emf will oppose this decrease by generating and induced magnetic flux that adds to the original flux. Lenz's law is one of the basic laws in electromagnetic induction for determining the direction of flow of induced currents and is related to the law of conservation of energy. According to the law of conservation of energy which states that the total amount of energy in the universe will always remain constant as energy can not be created nor destroyed. Lenz's law is derived from Michael Faraday's law of induction. One final comment about Lenz's Law regarding electromagnetic induction. We now know that when a relative motion exists between a conductor and a magnetic field, an emf is induced within the conductor.

But the conductor may not actually be part of the coils electrical circuit, but may be the coils iron core or some other metallic part of the system, for example, a transformer. The induced emf within this metallic part of the system causes a circulating current to flow around it and this type of core current is known as an Eddy Current. Eddy currents generated by electromagnetic induction circulate around the coils core or any connecting metallic components inside the magnetic field because for the magnetic flux they are acting like a single loop of wire. Eddy currents do not contribute anything towards the usefulness of the system but instead they oppose the flow of the induced current by acting like a negative force generating resistive heating and power loss within the core. However, there are electromagnetic induction furnace applications in which only eddy currents are used to heat and melt ferromagnetic metals.

EDDY CURRENTS CIRCULATING IN A TRANSFORMER



The changing magnetic flux in the iron core of a transformer above will induce an emf, not only in the primary and secondary windings, but also in the iron core. The iron core is a good conductor, so the currents induced in a solid iron core will be large. Furthermore, the eddy currents flow in a direction which, by Lenz's law, acts to weaken the flux created by the primary coil. Consequently, the current in the primary coil required to produce a given B field is increased, so the hysteresis curves are fatter along the H axis.



Eddy current and hysteresis losses can not be eliminated completely, but they can be greatly reduced. Instead of having a solid iron core as the magnetic core material of the transformer or coil, the magnetic path is "laminated". These laminations are very thin strips of insulated (usually with varnish) metal joined together to produce a solid core. The laminations increase the resistance of the iron-core thereby increasing the overall resistance to the flow of the eddy currents, so the induced eddy current power-loss in the core is reduced, and it is for this reason why the magnetic iron circuit of transformers and electrical machines are all laminated.

For more check:

Useful link: http://www.electronics-tutorials.ws/electromagnetism/electromagnetic-induction.html

For a useful video explaining the EM induction check:

Useful link: https://www.youtube.com/watch?v=3HyORmBip-w

AC GENERATOR WORKING PRINCIPLE:
For a useful video explaining the working principle of check this video:

Useful link: https://www.youtube.com/watch?v=gQyamjPrw-U