# Call for application for research scholarships

# for post-graduate international candidates

# RESEARCH PROJECT N. 24

**Title**

**Design of Energy-Efficient Hardware Accelerators for Deep Learning Applications**

**Scientific responsible (name, surname, role)**

Mario Roberto Casu, Associate Professor (mario.casu@polito.it)

**Short description of the research activity (max 250 words)**

The candidate will work on the design of an application-specific hardware accelerator for deep-learning applications aimed at very low power consumption. The target technology is 28-nm Fully-Depleted Silicon-on-Insulator (FDSOI) CMOS. The accelerator will be designed for working in a large voltage range (near-threshold to nominal voltage). The candidate will evaluate the possibility of applying a combination of standard low-power knobs like dynamic-voltage and frequency scaling (DVFS), as well as FDSOI-specific knobs like Reverse and Forward Body-Biasing (RBB & FBB). After evaluating the state of the art, the candidate will evaluate various alternatives (design-space exploration) using an analytical model for performance/throughput. The selected solution will be designed mostly at RT-level, although it is possible that a custom design will be needed for critical circuit blocks. The layout of the final circuit will be designed and the possibility for circuit fabrications will be evaluated (depending on the quality of final results).

**Specific requirements (experiences, skills)**

RTL design, VHDL or Verilog, microelectronics, Cadence (Virtuoso and Encounter), Synopsys (Design Compiler)

**Website of the research group (if any)**

**Keywords (min 3, max 6)**

Deep Learning, Application-Specific Integrated Circuits, Low-Power Design

**Research Area (max 1)**

Electronics, Control and Telecommunication Engineering