

**Call for application for research scholarships
for post-graduate international candidates**

RESEARCH PROJECT N. 29

Title

DESIGN OPTIMIZATION OF HIGH-SPEED LINKS VIA MACHINE LEARNING

Scientific responsible (name, surname, role)

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Short description of the research activity (max 250 words)

Machine learning has become a mature and powerful tool for solving problems in many different areas, including computational finance, image processing, energy forecasting and voice recognition. What is more important, the users can now rely on readily available state-of-the-art algorithms which are embedded in either open source or commercial software (e.g., Matlab). The typical application of the mentioned technique is however mainly related to classification problems, possibly involving heterogenous input data. The aim of the proposed activity is to carry out a first systematic analysis of the application of this class of algorithms to the parametric analysis and design optimization of realistic electronic links (e.g., a printed circuit board structure in a smartphone). The research work attempts bridging the gap between this promising solution and standard approaches. For the problem at hand the two steps involved are: (i) generate an efficient surrogate model for the response of the system under investigation as a function of the design parameters (e.g., the physical dimension of the interconnect); (ii) apply nature-inspired algorithms for the data link design optimization (e.g., for noise reduction). Emphasis is given on a systematic and unambiguous analysis of the performance of different techniques for the two items above.

Specific requirements (experiences, skills)

Basic knowledge of mathematics, statistics and probability. A course on operational research and optimization would be helpful.

Website of the research group (if any)

<http://www.emc.polito.it>

Keywords (min 3, max 6)

Electrical engineering, optimization tools, machine learning, system identification, circuit simulation, tolerance analysis

Research Area (max 1)

Electronics, Control and Telecommunication Engineering