PhD in Electrical, Electronics and Communications Engineering

Research Title: Circuits and Algorithms for IoT nodes Implementation

Funded by	Dipartimento di Elettronica e Telecomunicazioni (DET) Prof. Gianluca Setti

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Context of the research activity	The Internet of Things (IoT) is a rapidly emerging application space, poised to become the largest electronics market for the semiconductor industry. IoT devices are focused on sensing and actuating of the physical environment and aim to provide smart functionalities that would not be possible without the constant acquisition and exchange of information from/to the environment. Today, we begin to design and deploy smart grids, smart homes, smart water networks, smart transportation infrastructures, etc., that deeply rely on large aggregates of IoT nodes intertwining of diverse physical interactions and information processing. A key ingredient in IoT aggregates is their ability of autonomously gathering information about the real world by means of a potentially large number of sensing/acquisition/early processing nodes either embedded in objects or deployed ad-hoc. These nodes typically work on extremely low resource budgets in terms of available power, weight, etc. To limit their invasiveness with respect to the phenomena they observe, they

	communicate the acquired data wirelessly to the other elements of the IoT ensemble. Hence, ability of designing extremely parsimonious nodes is fundamental for the development of IoT systems. For example, ultra-low-power circuits for signal acquisition is fundamental for reducing energy signature, similarly low-level processing and elementary signal compression is sought to limit the data rate of the transmission that is often the main cause of power consumption. Aim of this project is to advance in this direction, exploiting innovative circuits/systems solutions.

Objectives	Objective of this research activity is to explore innovative solutions for the design and implementation of IoT nodes. Example of possible directions to explore are: 1) Implementation of Analog-to-Information Converters (AIC) Based on Compressed Sensing (CS). CS is a new paradigm for the acquisition/sampling of signals that violates the intuition behind the theorem of Nyquist-Shannon , so that, under surprisingly broad conditions, it is possible to reconstruct certain signals or images using far fewer samples or measurements than what required by traditional methods. Several architectures have been proposed for this, but none of them clearly show a significant advantaged in terms of energy consumption with respect to classical solution. One of the objective of the project will be the investigation of new AIC architectures based on algorithmic variation of standard SAR ADCs. Use of acquisition algorithm-hardware co-design techniques will be a key step for performance optimization. 2) Early feature detection in the compressed domain. When signals have been acquired by an IoT node, it would be certainly more efficient to extract the most important features from them in order both to take early decision (f.i. triggering an alarm in case of a malfunction of the device monitored by the IoT node) and to transmit only the key features necessary for managing the particular task at hand. Objective of this activity is to develop a suite of (possibly machine learning based) feature extraction and classification algorithms able to be applied to different tasks (such has the detection of hear fibrillation, or of structural integrity anomaly). 3) In memory computing. From a hardware-based point of view, data analysis consists of three components: the processor and the related memory to perform the calculations, the storage necessary to collect the (elaborated) data, and the system that transfer the

	information between the first two. Of course, the latency of the slowest (sub)systems determines the overall system performance, and this is, nowadays, the one of storage. In-memory computing is an attractive approach for performing computationally expensive tasks of a high-level algorithm in an energy-efficient manner by moving the required data from storage into random access memory. For instance, crossbar arrays of resistive memory (memristive) devices can be used to store a matrix and perform analog matrix-vector multiplications at constant O(1) time complexity without intermediate movements of data. This capability has been exploited in a wide range of applications from neural network inference to solving systems of linear equations. One of the objectives of the project could be to use a similar technique to perform CS acquisition in an IoT nodes.

Skills and competencies for the development of the activity	The candidate must be familiar with integrated circuit design (both digital and analog) and related CAD tools (mainly Cadence/Synopisis). Acquaintance with digital programmable devices such as DSPs, microcontrollers and/or FPGAs, with particular reference to the efficient programmability of I/O modules for the sake of test signal generation/acquisition. Capability of master theoretical subjects (related to signal processing algorithms in particular) as well as capabilities of implementing circuits/systems.