PhD in Electrical, Electronic and Telecommunications Engineering

Research Title: Ultra-low power, non-conventional integrated circuits for the Internet of Things

SESSION: SUMMER 2019

Funded by	Dipartimento di Elettronica e Telecomunicazioni (DET) Proff. P. Crovetti, F. Musolino, F. Gregoretti

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Context of the research activity	Unlike digital integrated circuits (ICs), analog and mixed-signal ICs do not take advantage of CMOS technology scaling and are becoming more and more often the bottleneck in terms of cost, power consumption and performance of nano-scale integrated circuits and systems. In view of that, alternative, mostly digital solutions and IC design approaches suitable to replace traditional analog circuits are highly demanded to address the tight requirements of performance, configurability, ultra-low power consumption of interfaces, acquisition front ends and power management blocks for Internet of Things (IoT) applications. In particular, unconventional circuit- and architecture-level design techniques, which are challenging the traditional separation of analog and digital domains in favor of a unified, cross-domain vision of information acquisition and processing circuits, are emerging in recent years. Such techniques will be intensively investigated in the framework of this research and will be extensively applied to design novel integrated circuits targeting the requirements of IoT applications.

Objectives	The research is focused on the development of digital-in-concept, ultra-low-power, reconfigurable integrated circuits for signal acquisition (including, but not limited to, sensor acquisition front-ends, baseband A/D and D/A data converters, analog to information converters) and power management (e.g. digital low dropout regulators (LDOs), reference circuits) targeting the requirements of present-day and future Internet of Things (IoT) applications. For this purpose, non-conventional approaches suitable to associate and to retrieve information to/from baseband electrical signals will be explored to overcome the limitation of nanoscale transistors and to allow the integration of traditional analog functions in a fully digital flow. More specifically, the research activity will cover the full design flow of integrated circuits implementing novel solutions and signal/power processing concepts in a nano-scale CMOS technology, including: - theoretical assessment and high-level simulation of innovative signal processing concepts; - high-level architectural design of circuits based on the novel concepts, design space exploration and FPGA prototyping (when applicable); - transistor level design and simulation and performance optimization (Cadence environment); - layout generation, post-layout simulations and integration on silicon (Cadence environment); - experimental characterization of the prototypes and analysis of the experimental results

Skills and competencies for the development of the activity	A good familiarity with the Analog-Mixed Signal and/or Digital and/or RF CMOS IC concepts and design flow are expected. Moreover, a deep understanding of conventional data conversion and signal processing techniques is required. Familiarity with Matlab and Cadence environments are also required.