CCE_5

Title of the doctoral program

Computer and control engineering

Title of the research activity

Methods and Instruments for the characterization of Integrated Circuits during Reliability testing

Short description of the research activity

Nowadays, it is continuously growing the number of integrated circuits included in critical environments such as the automotive and the avionic. For this reason, semiconductor manufacturer has to guarantee the reliability of the released components for the entire life-cycle that can be up to 10 -15 years.

Commonly, the measurement of the reliability of an IC is done by using Burn-In and Reliability testers. Such instrument permits to accelerate the obsolescence of a component by running suitable test up to limit conditions such as high temperature, high voltages, high frequencies. This type of operation is normally called stress/test and it is performed on a variable number of ICs (up to some thousands) both at wafer or package level.

Short stress/test duration allows discarding those components that would exhibit a early failure during their mission, and permits to mitigate the so called infant mortality. This hypothesis is based on a failure distribution model known as “bathtub curve”, which indicates that ICs showing a good behavior after an initial stress period will work correctly for the rest of their life cycle. On the contrary, long stress/test times permits to evaluate the length of the IC life cycle.

The validity of the bathtub curve has been recently discussed by semiconductor producers, which underline how the performance, and therefore the reliability, of a manufactured IC in the nanometric domain may decrease differently than predicted.

For the reliability sakes in this field, it is mandatory to adopt effective mechanisms that allows to

1. extract failure information during the stress/test activity without impacting its efficiency
2. store the failure information that may derive from the analysis of a large number of devices
3. interpret the obtained results, possibly relating failures with the manufacturing technology returning indication of those aspects that can be improved during realization.

Frameworks

1. *Failure information extraction during stress/test*

Work related to this aspect of the problematic can divides in two parts:

a. Design of a SW platform for Design-for-Test and Design-for-Diagnosis structures insertion in IC design in order to retrieve precise information on faulty components
b. Embedded Operative System optimization to perform data collection without impacting the stress/test time

2. *Information storage*

Design and realization of Database suitable to store the downloaded information and whose structure suits for a large number of measure type and temporal information.

3. *Result interpretation*

Design of a SW platform that elaborated the failure information wrote in the DB to provide the following information:

a. The temporal progression of failures
b. The set of possible location of systematic problems along the various stress types

c. The statistical analysis of failures over IC groups

Expected results

General issues.

Development of a multi-disciplinary platform that includes SW engineering, embedded operative systems and database aspects and oriented to the reliability characterization of ICs

Industrial issues.

Identification of failure mechanisms due to obsolescence and remodeling of the bathtub curve for nanometric technologies

Optimization of reliable test equipments, in particular concerning the operative system.

Academic issues.

Dissemination in the following fields:

a. Design-for-Diagnosis
b. Automatic generation of diagnostic patterns oriented to nanometric fault models
c. Efficiency of the stress/test process
d. Diagnostic information Data mining
e. Statistical interpretation of diagnostic data over large IC groups.

Scientific responsible (name, surname, role, email)

Paolo Bernardi, Assistant professor, paolo.bernardi@polito.it

Number of vacancies for XXXI cycle (3 years program)

1

Specific requirements (experiences, skills)

VHDL, Verilog, Simulation, Compilers and Debugger, Database, Operative Systems

Website of the research group (if any)

www.cad.polito.it