CCE_8

Title of the doctoral program

Computer and control engineering

Title of the research activity

Adaptive storage-class-memory (SCM)

Short description of the research activity

In today CMOS the short-comings caused by technology scaling are becoming more relevant than the benefits. The memory capacity increases at the cost of high reliability issues, large power consumption, with no substantial performance improvement. To overcome these shortcomings, novel memory devices are being currently under research, to identify the best candidate to replace today charge based memories. Amongst these, the most promising so far, are the resistive RAM and the magnetic RAM. Emerging storage-class memories (SCM) promise to change many assumptions about storage. They have the persistence and density of storage but the fine-grained access of memory. The research activity will be focused on magnetic RAM based Storage-Class-Memory design, targeting low power consumption, high reliability, high speed and high density. In this project, methodologies and mechanisms for improving the adaptability and reliability of the memory will be developed and implemented at circuit level (both analog and digital modules will be targeted). Methodologies for dynamic reconfiguration of the SCM memory system will be devised, starting from the analysis of the physical degrees of freedom. The developed memory system should offer currently non-existing flexibility features, without compromising performance, power, and reliability.

Scientific responsible (name, surname, role, email)

Paolo Prinetto, Full Professor, paolo.prinetto@polito.it

Number of vacancies for XXXI cycle (3 years program)

1

Specific requirements (experiences, skills)

Analog and Digital Design

Website of the research group (if any)

www.testgroup.polito.it